Power Amplifiers

3.1 General Concepts:

A ***power amplifier*** is one that is designed to deliver a large amount of power to a load. To perform this function, a power amplifier must itself be capable dissipating large amounts of power; so that the heat generated when it is operated at high current and voltage levels is released into the surroundings at a rate fast enough to prevent destructive temperature buildup. Power amplifiers typically contain bulky components having large surface areas to enhance heat transfer to the environment. A power transistor is a discrete device with a large surface area and a metal case.

A power amplifier is often the last stage of an amplifier system designed to modify signal characteristics referred to as signal conditioning. It is designed at least one of its semiconductor components, typically a power transistor, can be operated over substantially the entire range of its output characteristics, from saturation to cutoff. This mode of operation is called ***large-signal operation***. The term "large-signal operation" is also applied to devices used in digital switching circuits. In these applications, the output level switches between "high" and "low" (cutoff and saturation), but remains in those states most of the time. Power dissipation is therefore not a problem. On the other hand, the variations in the output level of a power amplifier occur in the active region, between the two extremes of saturation and cutoff, so a substantial amount of power is dissipated.

3.2 Transistor Power Dissipation:

A power is the rate at which energy is consumed or dissipated (1 watt = 1 joule/second). If the rate at which heat energy is dissipated in a device is less than the rate at which it is generated, the temperature of the device must rise. In electronic devices, electrical energy is converted to heat energy at a rate given by $P = VI$ watts, and temperature rises when this heat energy is not removed at a comparable rate. Since semiconductor material is irreversibly damaged when subjected to temperatures beyond a certain limit, temperature is the parameter that ultimately limits the amount of power a semiconductor device can handle.

Transistor manufacturers specify the maximum permissible junction temperature and the maximum permissible power dissipation that a transistor can withstand. In normal transistor operation, the collector-base junction is reverse biased and has, on average, a large voltage across it, while the base-emitter junction has a small forward-biasing voltage. Consequently, most of the heat generated in a transistor is produced at the collector-base junction. The total power dissipated at the junctions is

$$P_d = v_{cb}i_c + v_{be}i_e \approx (v_{cb} + v_{be})i_c \approx v_{ce}i_c.$$

Fig. 3-1 shows a simple common-emitter amplifier and its dc load line plotted on I_C–V_{CE} axes. As the amplifier output changes in response to an input signal, the collector current and voltage undergo variations along the load line and intersect different hyperbolas of power dissipation. It is clear that the power dissipation changes as the amplifier output changes. For safe operation, the load line must lie below and to the left of the hyperbola corresponding to the maximum permissible power dissipation.

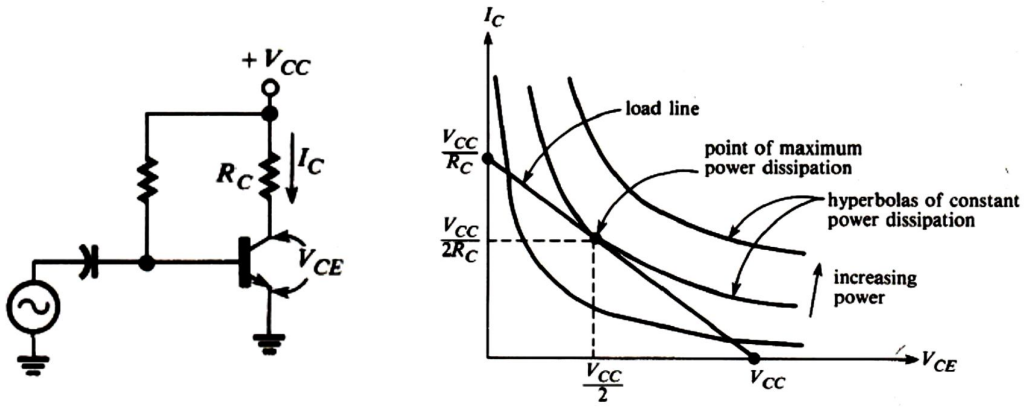


Fig. 3-1

It can be shown that the point of maximum power dissipation occurs at the center of the load line, where $V_{CE} = V_{CC}/2$ and $I_C = V_{CC}/2R_C$ (see Fig. 3-1). Therefore, the maximum power dissipation is

$$P_d(\text{max}) = \left(\frac{V_{CC}}{2}\right)\left(\frac{V_{CC}}{2R_C}\right) = \frac{V_{CC}^2}{4R_C} \qquad [3\text{-}1]$$

To ensure that the load line lies below the hyperbola of maximum dissipation, we therefore require that

$$\frac{V_{CC}^2}{4R_C} < P_d(\text{max}) \quad \Rightarrow$$

$$R_C > \frac{V_{CC}^2}{4P_d(\text{max})} \qquad [3\text{-}2]$$

where P_d(max) is the manufacturer's specified maximum dissipation at a specified ambient temperature.

Exercise 3-1:

The amplifier in Fig. 3-1 is to be operated with $V_{CC} = 20$V and $R_C = 1$ kΩ.

(a) What maximum power dissipation rating should the transistor have?

(b) If an increase in ambient temperature reduces the maximum rating found in (a) by a factor of 2, what new value of R_C should be used to ensure safe operation?

[Answers: (a) 0.1 W, (b) 2 kΩ]

3.3 Class-A Power Amplifiers:

All the small-signal amplifiers have been designed so that output voltage can vary in response to both positive and negative inputs; that is, the amplifiers are biased so that under normal operation the output never saturates or cuts off. An amplifier that has that property is called a ***class-A*** amplifier. More precisely, an amplifier is class A if its output remains in the active region during a complete cycle (one full period) of a sine-wave input signal.

Fig. 3-2 shows a typical class-A amplifier and its input and output waveforms. In this case, the transistor is biased at $V_{CE} = V_{CC}/2$, which is midway between saturation and cutoff, and which permits maximum output voltage swing. The output can vary through (approximately) a full V_{CC} volts, peak-to-peak. The output is in the transistor's active region during a full cycle (360°) of the input sine wave.

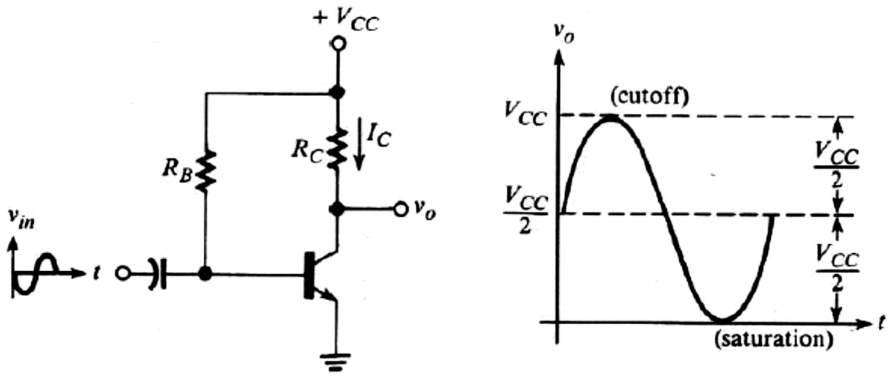


Fig. 3-2

The ***efficiency*** of a power amplifier is defined to be

$$\eta = \frac{\text{average signal power delivered to load}}{\text{average power drawn from dc source}} \qquad [3\text{-}3]$$

The numerator of Eqn. [3-3] is average signal power, that is, average ac power, excluding any dc or bias components in the load. Recall that when voltages and currents are sinusoidal, average ac power can be calculated using any of the following relations:

$$P = V_{rms}I_{rms} = V_P I_P/2 = V_{PP}I_{PP}/8$$
$$P = I_{rms}^2 R = I_P^2 R/2 = I_{PP}^2 R/8 \qquad [3\text{-}4]$$
$$P = V_{rms}^2/R = V_P^2/2R = V_{PP}^2/8R$$

The efficiency of a class-A amplifier is 0 when no signal is present. The amplifier is said to be in standby when no signal is applied to its input. We will now derive a general expression for the efficiency of the class-A amplifier shown in Fig. 3-2. In doing so, we will not consider the small power consumed in the base-biasing circuit, i.e., the power at the input side: $I_B^2 R_B + v_{be} i_b$.

3.3.1 Series-Fed Class-A Power Amplifiers:

Fig. 3-3 shows the voltages and currents used in our analysis. Notice that resistance R is considered to be the load. We will refer to this configuration as a ***series-fed*** class-A amplifier, and we will consider ***capacitor-*** and ***transformer-coupled*** loads in a later discussion.

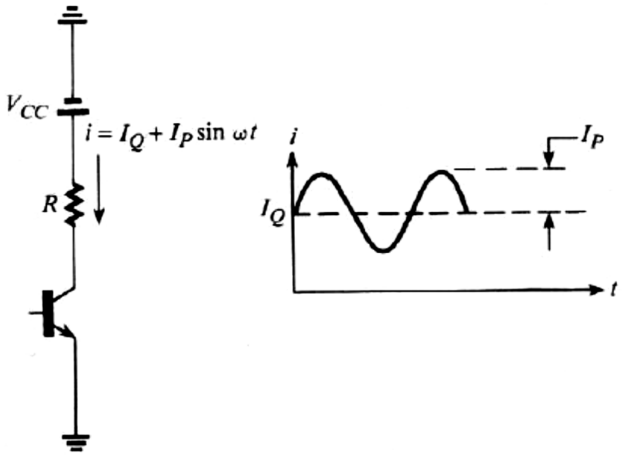


Fig. 3-3

The instantaneous power from the dc supply is

$$P_S(t) = V_{CC}i = V_{CC}(I_Q + I_P \sin \omega t) = V_{CC}I_Q + V_{CC}I_P \sin \omega t.$$

Since the average value of the sine term is 0, the average power from the dc supply is

$$P_S = V_{CC}I_Q.$$

The average signal power in load resistor R is, from Eqn. [3-4],

$$P_R = I_P^2 R/2 .$$

Therefore, by Eqn. [3-3],

$$\eta = \frac{P_R}{P_S} = \frac{I_P^2 R}{2V_{CC}I_Q} \qquad [3\text{-}5]$$

We see again that the efficiency is 0 under no-signal conditions ($I_P = 0$) and that efficiency rises as the peak signal level I_P increases. The maximum possible efficiency occurs when I_P has its maximum possible value without distortion. When the bias point is at the center of the load line, as shown in Fig. 3-1, the quiescent current is one-half the saturation current, and the output current can swing through the full range from 0 to V_{CC}/R amps without distorting (clipping). Thus, the maximum undistorted peak current is also one-half the saturation current:

$$I_Q = I_P = V_{CC}/2R.$$

Substituting this equation into Eqn. [3-5], we find the maximum possible efficiency of the series-fed, class-A amplifier:

$$\eta(\text{max}) = \frac{(V_{CC}/2R)^2 R}{2V_{CC}(V_{CC}/2R)} = 0.25$$

This result shows that the best possible efficiency of a series-fed, class-A amplifier is undesirably small: only 1/4 of the total power consumed by the circuit is delivered to the load, under optimum conditions. For that reason, this type of amplifier is not widely used in heavy power applications. The principal advantage of the class-A amplifier is that it generally produces less signal distortion than some of the other, more efficient classes that we will consider later.

Another type of efficiency used to characterize power amplifiers relates signal power to total power dissipated at the collector. Called ***collector efficiency***, its practical significance stems from the fact that a major part of the cost and bulk of a power amplifier is invested in the output device itself and the means used to cool it. Therefore, it is desirable to maximize, the ratio of signal power in the load to power consumed by the device. Collector efficiency η_c is defined by

$$\eta_c = \frac{\text{average signal power delivered to load}}{\text{average power dissipated at collector}} \qquad [3\text{-}6]$$

The average power P_C dissipated at the collector of the class-A amplifier in Fig. 3-3 is the product of the dc (quiescent) voltage and current:

$$P_C = V_Q I_Q = (V_{CC} - I_Q R)I_Q.$$

Therefore,

$$\eta_c = \frac{I_P^2 R/2}{(V_{CC} - I_Q R)I_Q} \qquad [3\text{-}7]$$

The maximum value of η_c occurs when I_P is maximum, $I_P = I_Q = V_{CC}/2R$, as previously discussed. Substituting these values into Eqn. [3-7] gives

$$\eta_c(\text{max}) = \frac{(V_{CC}/2R)^2 R/2}{(V_{CC} - V_{CC}/2)V_{CC}/2R} = 0.5$$

3.3.2 Capacitor-Coupled Class-A Power Amplifiers:

Fig. 3-4 shows the output side of a class-A amplifier with capacitor-coupled load R_L. Also shown are the dc and ac load lines that result. In this case, the average power delivered to the load is

$$P_L = I_{PL}^2 R_L/2,$$

where I_{PL} is the peak ac load current. The average power from the dc source is computed in the same way as for the series-fed amplifier: $P_S = V_{CC}I_Q$, so the efficiency is

$$\eta = \frac{I_{PL}^2 R_L}{2V_{CC}I_Q} \qquad [3\text{-}8]$$

As in the case of the series-fed amplifier, the efficiency is 0 under no-signal (standby) conditions and increases with load current I_{PL}.

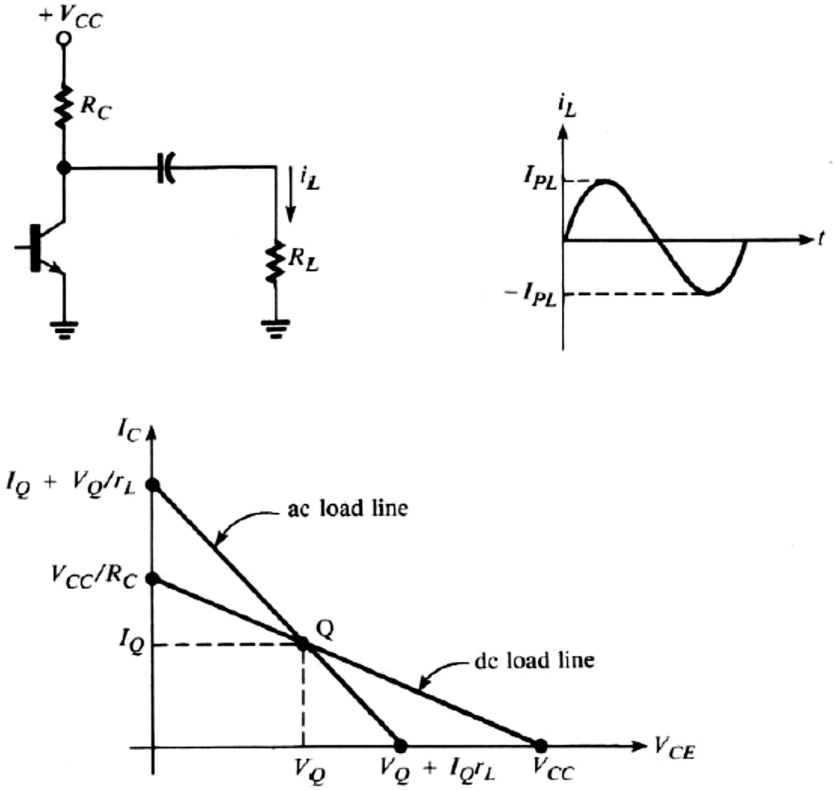


Fig. 3-4

Recall that maximum output swing can be achieved by setting the Q-point in the center of the ac load line, at

$$I_Q = \frac{V_{CC}}{R_C + r_L}.$$

The peak collector current under those circumstances is $V_{CC}/(R_C + r_L)$. Neglecting the transistor output resistance, the portion of the collector current that flows in R_L is, by the current-divider rule,

$$I_{PL} = \left(\frac{V_{CC}}{R_C + r_L}\right)\left(\frac{R_C}{R_C + R_L}\right).$$

The average ac power in the load resistance R_L is then

$$P_L = \frac{I_{PL}^2 R_L}{2} = \left[\left(\frac{V_{CC}}{R_C + r_L}\right)\left(\frac{R_C}{R_C + R_L}\right)\right]^2 (R_L/2).$$

The average power supplied from the dc source is

$$P_S = V_{CC} I_Q = \frac{V_{CC}^2}{R_C + r_L}.$$

Therefore, the efficiency under the conditions of maximum possible undistorted output is

$$\eta = \frac{P_L}{P_S} = \frac{\left[\left(\frac{V_{CC}}{R_C + r_L}\right)\left(\frac{R_C}{R_C + R_L}\right)\right]^2 (R_L/2)}{\frac{V_{CC}^2}{R_C + r_L}} \Rightarrow$$

$$\eta = \frac{R_C R_L}{2(R_C + 2R_L)(R_C + R_L)} = \frac{r_L}{2(R_C + 2R_L)} \qquad [3\text{-}9]$$

Eqn. [3-9] shows that the efficiency depends on both R_C and R_L. In practice, R_L is a fixed and known value of load resistance, will the value of R_C is selected by the designer. Using calculus (differentiating Eqn. [3-9] with respect to R_C), it can be shown that η is maximized by setting $R_C = \sqrt{2} R_L$. With this value of R_C, the maximum efficiency is

$$\eta(\text{max}) = 0.0858$$

Another criterion for choosing R_C is to select its value so that maximum power is transferred to the load. Since the transistor output resistance has been neglected, maximum power transfer occurs when $R_C = R_L = R$. Under that circumstance, $r_L = R/2$, and, by substituting into Eqn. [3-9], we find the maximum possible efficiency with maximum power transfer to be

$$\eta(\text{max}) = 0.0833 \quad \text{(max power transfer)}.$$

It is interesting to note that the efficiency under maximum power transfer (0.0833) is somewhat less than that which can be achieved (0.0858) without regard to power transfer. In either case, the maximum efficiency is substantially less than that attainable in the series-fed class-A amplifier.

Exercise 3-2:

The class-A amplifier shown in Fig. 3-5 is biased at V_{CE} = 12 V. The output voltage is the maximum possible without distortion. Find

(a) the average power from the dc supply,
(b) the average power delivered to the load,
(c) the efficiency, and
(d) the collector efficiency.

[Answers: (a) 5.76 W, (b) 0.36 W, (c) 0.0625, (d) 0.125]

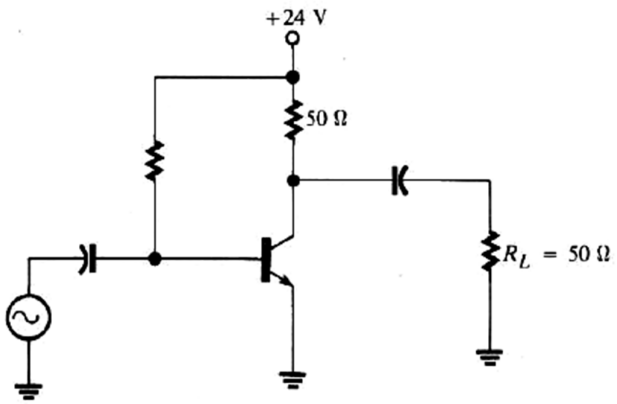


Fig. 3-5

3.3.3 Transformer-Coupled Class-A Power Amplifiers:

Output transformers are used to couple power amplifiers to their loads. As in other coupling applications, the advantages of a transformer are that it provides an opportunity to achieve impedance matching for maximum power transfer and that it blocks the flow of dc current in a load.

Fig. 3-6 shows a transformer used to couple the output of a transistor to load R_L. Also shown are the dc and ac load lines for the amplifier. Here we assume that the dc resistance of the primary winding is negligibly small, so the dc load line is vertical (slope = $-1/R_{dc} = -\infty$). Recall that the ac resistance r_L reflected to the primary side is

$$r_L = (N_p/N_s)^2 R_L \qquad [3\text{-}10]$$

where N_p and N_s, are the numbers of turns on the primary and secondary windings, respectively. As shown in the figure, the slope of the ac load line is $-1/r_L$.

Since we are assuming that there is negligible resistance in the primary winding, there is no dc voltage drop across the winding, and the quiescent collector voltage is therefore V_{CC} volts, as shown in Fig. 3-6. Conventional base-bias circuitry (not shown in the figure) is used to set the quiescent collector current I_Q. The Q-point is the point on the dc load line at which the collector current equals I_Q.

Since V_{CE} cannot be negative, the maximum permissible decrease in V_{CE} below its quiescent value is $V_Q = V_{CC}$ volts. Thus, the maximum possible peak value of V_{CE} is V_{CC} volts. To achieve maximum peak-to-peak output variation, the intercept of the ac load line on the V_{CE}-axis should therefore be $2V_{CC}$ volts, as shown in Fig. 3-6. The quiescent current I_Q is selected so that the ac load line, a line having slope $-1/r_L$, intersects the V_{CE}-axis at $2V_{CC}$ volts.

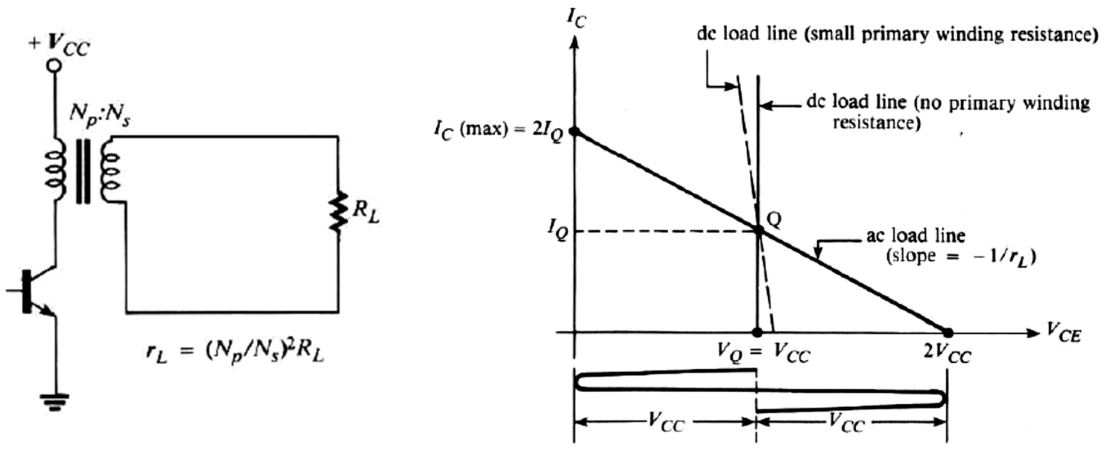


Fig. 3-6

The ac load line intersects the I_C-axis in Fig. 3-6 at I_C(max). There is no theoretical limit to the value that I_C may have, since there is no limiting resistance in the collector circuit. However, in practice, I_C must not exceed the maximum permissible collector current for the transistor and it must not be so great that the magnetic flux of the transformer saturates. When the transformer saturates, it can no longer induce current in the secondary winding and signal distortion results. When I_Q is set for maximum signal swing (so that $V_{CE}(\text{max}) = 2V_{CC}$), I_Q is one-half I_C(max); that is, $I_C(\text{max}) = 2I_Q$, as shown in Fig. 3-6. Thus, the maximum values of the peak primary voltage and peak primary current

are V_{CC} and I_Q, respectively. Since the ac output can vary through this range, below and above the quiescent point, the amplifier is of the class-A type.

Unlike the case of the capacitor-coupled or series-fed amplifier, the collector voltage can exceed the supply voltage. A transistor having a collector breakdown voltage equal to at least twice the supply voltage should be used in this application.

The ac power delivered to load resistance R_L in Fig. 3-6 is

$$P_L = \frac{V_s^2}{2R_L} = \frac{V_{PL}^2}{2R_L},$$

where $V_s = V_{PL}$ is the peak value of the secondary, or load, voltage. The average power from the dc supply is

$$P_S = V_{CC} I_Q.$$

Therefore, the efficiency is

$$\eta = \frac{P_L}{P_S} = \frac{V_{PL}^2}{2R_L V_{CC} I_Q} \qquad [3\text{-}11]$$

Under maximum signal conditions, the peak primary voltage is V_{CC} volts, so the peak load voltage is

$$V_{PL} = (N_s/N_p)V_{CC}.$$

Also, since the slope of the ac load line is $-1/r_L$, we have

$$\frac{|\Delta I_C|}{|\Delta V_{CE}|} = \frac{1}{r_L} = \frac{I_Q}{V_Q} \Rightarrow$$

$$I_Q = \frac{V_Q}{r_L} = \frac{V_{CC}}{(N_p/N_s)^2 R_L}.$$

Substituting the maximum values of V_{PL} and I_Q into Eqn. [3-11], we find the maximum possible efficiency of the transformer-coupled class-A amplifier:

$$\eta(\max) = \frac{(N_s/N_p)^2 V_{CC}^2}{(2R_L V_{CC}) \frac{V_{CC}}{(N_p/N_s)^2 R_L}} = 0.5$$

The maximum efficiency is twice that of the series-fed class-A amplifier and six times that of the capacitor-coupled class-A amplifier. This improvement in efficiency is attributable to the absence of external collector resistance that would otherwise consume dc power. The collector efficiency of the transformer-coupled class-A amplifier is the same as the overall amplifier efficiency, because the average power from the dc supply is the same as the collector dissipation:

$$P_S = V_{CC} I_Q = V_Q I_Q = P_C.$$

In practice, a full output voltage swing of $2V_{CC}$ volts cannot be achieved in a power transistor. The device is prevented from cutting off entirely by virtue of a relatively large leakage current, and it cannot be driven all the way into saturation ($I_C = I_C(\max)$) without creating excessive distortion.

Exercise 3-3:

The transistor in the power amplifier shown in Fig. 3-7(a) has the output characteristics shown in Fig. 3-7(b). Assume that the transformer has zero resistance.

(a) Construct the (ideal) dc and ac load lines necessary to achieve maximum output voltage swing. What quiescent values of collector and base current are necessary to realize the ac load line?

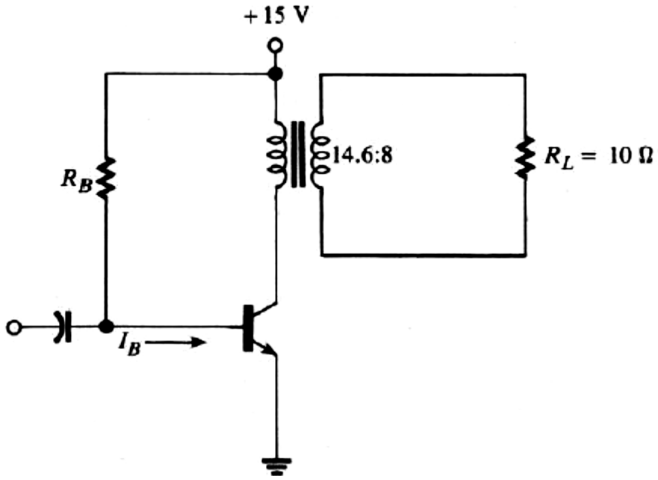
(b) What is the smallest value of $I_C(\max)$ for which the transistor should be rated?

(c) What is the maximum peak-to-peak collector voltage, and what peak-to-peak base current is required to achieve it? Assume that the base current cannot go negative and that, to minimize distortion, the collector should not be driven below 2.5 V in the saturation region.

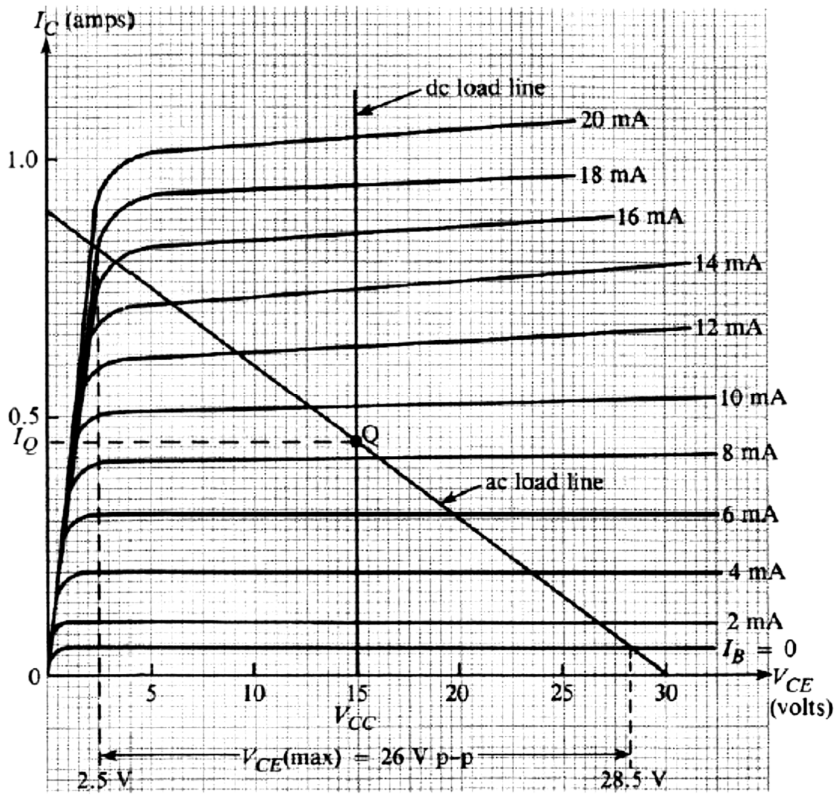
(d) Find the average power delivered to the load under the maximum signal conditions of part (c).

(e) Find the power dissipated in the transistor under no-signal conditions (standby).

(f) Find the efficiency.



(a)



(b)

Fig. 3-7

The Solution to Exercise 3-3:

(a) The vertical dc load line intersects the V_{CE}-axis at V_{CC} = 15 V, as shown in Fig. 3-7(b). To find the slope of the ac load line, we must find r_L. From Eqn. [3-10], $r_L = (N_p/N_s)^2 R_L = (14.6/8)^2(10) = 33.3\ \Omega$.
Thus, the slope of the ac load line is $-1/r_L = -1/33.3 = -0.03$ A/V. To achieve the ideal maximum output swing, we want the ac load line to intercept them V_{CE}-axis at $2V_{CC}$ = 30 V. Since the slope of that line has magnitude 0.03, it will intercept the I_C-axis at I_C = (0.03) (30) = 0.9 A. The ac load line is then drawn between the two intercepts (0 A, 30 V) and (0.9 A, 0 V), as shown in Fig. 3-7(b).
The ac load line intersects the dc load line at the Q-point. The quiescent collector current at that point is seen to be I_Q = 0.45 A. The corresponding base current is approximately halfway between I_B = 8 mA and I_B = 10 mA, so the quiescent base current must be 9 mA.

(b) The maximum collector current is I_C(max) = 0.9 A, at the intercept of the ac load line on the I_C-axis. Actually, we will not operate the transistor that far into saturation, since we do not allow V_{CE} to fall below 2.5 V. However, a maximum rating of 0.9 A (or 1 A) will provide us with a margin of safety.

(c) The maximum value of V_{CE} occurs on the ac load line at the point where I_B = 0. As shown in Fig. 3-7(b), this value is 28.5 V. Since the minimum permissible value of V_{CE} is 2.5 V, the maximum peak-to-peak voltage swing is 28.5 − 2.5 = 26 Vp-p. As can be seen on the characteristic curves, the base current must vary from I_B = 0 to I_B = 18 mA, or 18 mA peak-to-peak, to achieve that voltage swing.

(d) The peak primary voltage in the transformer is (l/2) (26) = 13 V. Therefore the peak secondary, or load voltage is $V_{PL} = (N_s/N_p)\ V_{P(\text{primary})}$ = (8/14.6) (13) = 7.12 V. The average load power is then
$P_L = \frac{V_{PL}^2}{2R_L} = \frac{(7.12)^2}{20} = 2.53$ W.

(e) The standby power dissipation is $P_d = V_Q I_Q = V_{CC} I_Q$ = (15) (0.45) = 6.75 W.

(f) The standby power dissipation found in part (e) is the same as the average power supplied from the dc source, so
η = 2.53/6.75 = 0.375
Question: Why is this value less than the theoretical maximum of 0.5?

3.4 Class-B Power Amplifiers:

Transistor operation is said to be class B when output current varies during only one half-cycle of a sine-wave input. In other words, the transistor is in its active region, responding to signal input, only during a positive half-cycle or only during a negative half-cycle of the input. This operation is illustrated in Fig. 3-8. In practical amplifiers, two transistors are operated class B: one to amplify positive signal variations and the other to amplify negative signal variations. The amplifier output is the composite waveform obtained by combining the waveforms produced by each class-B transistor. An amplifier utilizing transistors that are operated class B is called a class-B amplifier.

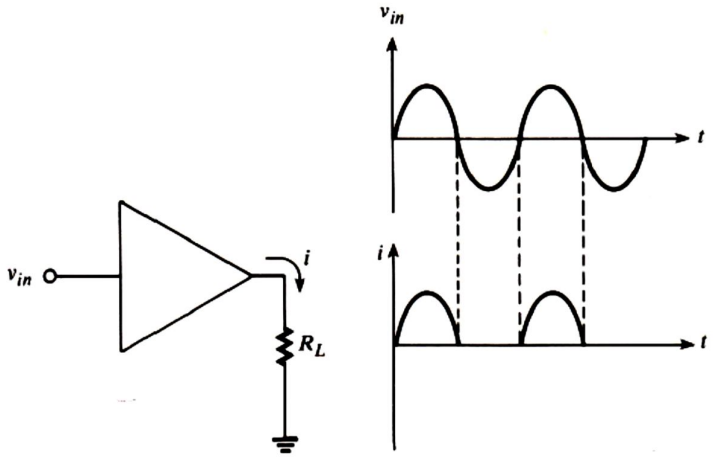


Fig. 3-8

3.4.1 Push-Pull Amplifiers:

A push-pull amplifier uses two output devices to drive a load. The name is derived from the fact that one device is primarily (or entirely) responsible for driving current through the load in one direction (pushing), while the other device drives current through the load in the opposite direction (pulling). The output devices are typically two transistors, each operated class B, one of which conducts only when the input is positive, and the other of which conducts only when the input is negative. This arrangement is called a class-B, push-pull amplifier and its principle is illustrated in Fig. 3-9.

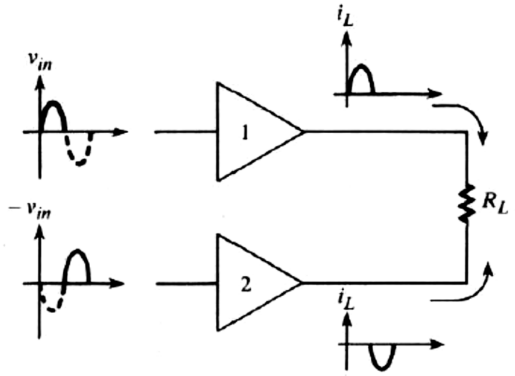


Fig. 3-9

In Fig. 3-9 that amplifying devices 1 and 2 are driven by equal-amplitude, out-of-phase input signals. The signals are identical except for phase. Here we assume that each device conducts only when its input is positive and is cut off when its input is negative. The net effect is that device 1 produces load current when the input is positive and device 2 produces load current, in the opposite direction, when the input is negative. An example of a device that has the property that it produces output (collector) current only when its input (base-to-emitter) voltage is positive is an NPN transistor having no base biasing circuitry, that is, one that is biased at cutoff. As we shall see, NPN transistors can be used as the output amplifying devices in push-pull amplifiers. However, the circuitry must be somewhat more elaborate than that diagrammed in Fig. 3-9, since we must make provisions for load current of low through a complete circuit, regardless of current direction. Obviously, when amplifying devise 1 in Fig. 3-9 is cut off, it cannot conduct current produced by device 2, and vice versa.

3.4.2 Push-Pull Amplifiers with Output Transformers:

Fig. 3-10 shows a push-pull arrangement that permits current to flow in both directions through a load even though one or the other of the amplifying devices (NPN transistors) is always cut off. The output transformer shown in the figure is the key component. The primary winding is connected between the transistor collectors and that its center tap is connected to the dc supply, V_{CC}. The center tap is simply an electrical connection made at the center of the winding, so there are an equal number of turns between each end of the winding and the center tap. The figure does not show the push-pull driver circuitry, which must produce out-of-phase signals on the bases of Q_1 and Q_2.

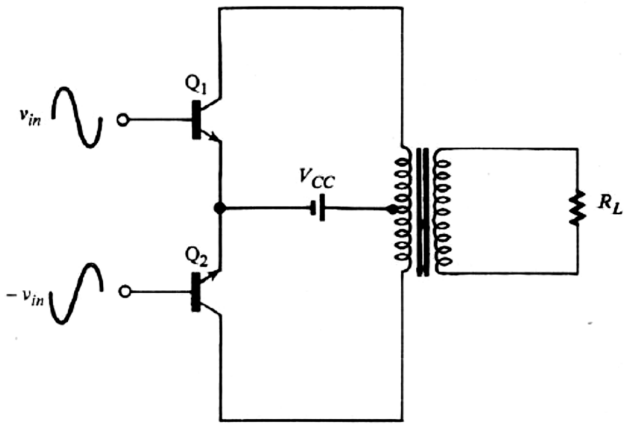
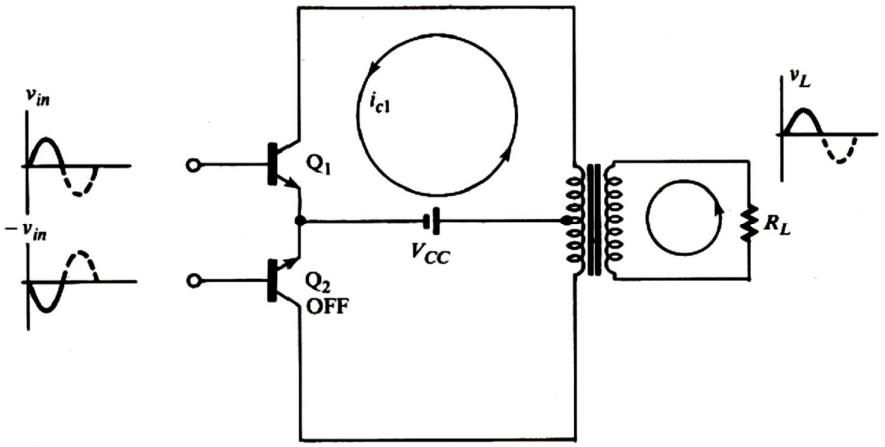


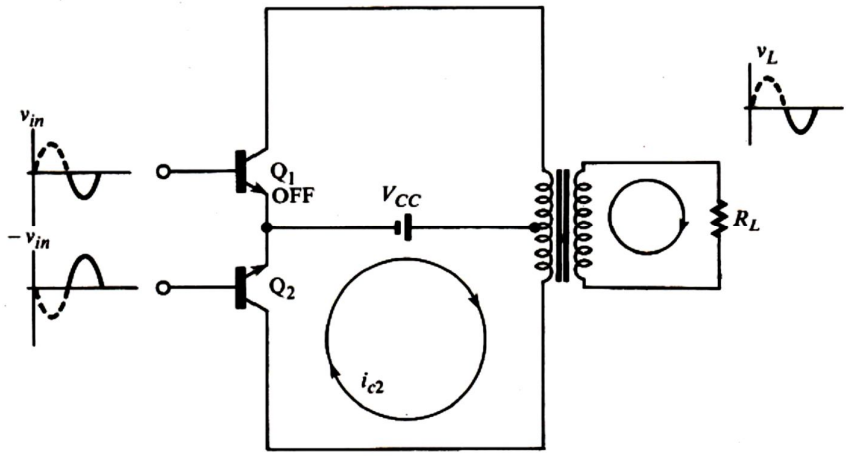
Fig. 3-10

Fig. 3.11 shows how current flows through the amplifier during a positive half-cycle of input and during a negative half-cycle of input. In Fig. 3.11(a), the input to Q_1 is the positive half-cycle of the signal, and since the input to Q_2 is out-of-phase with that to Q_1, Q_2 is driven by a negative half-cycle. Neither class-B transistor is biased. Consequently, the positive base voltage on Q_1 causes it to turn on and conduct current in the counterclockwise path shown. The negative base voltage on Q_2 keeps that transistor cut off. Current flowing in the upper half of the transformer's primary induces current in the secondary, and current flows through the load.

In Fig. 3.11(b), the input signal on the base of Q_1 has gone negative, so its inverse on the base of Q_2 is positive. Therefore, Q_2 conducts current in the clockwise path shown, and Q_1 is cut off. Current induced in the secondary winding is in the direction opposite that shown in Fig. 3-11(a). The upshot is that current flows through the load in one direction when the input signal is positive and in the opposite direction when the input signal is negative, just as it should in an ac amplifier.



(a)



(b)

Fig. 3-11

Fig. 3-12 displays current flow in the push-pull amplifier in the form of a timing diagram. Here the complete current waveforms are shown over two full cycles of input. For purposes of this illustration, counterclockwise current (in Fig. 3-11) is arbitrarily assumed to be positive and clockwise current is therefore negative. As far as the load is concerned, current flows during the full 360º of input signal. Fig. 3-12(e) shows that the current i_S from the power supply varies from 0 to the peak value I_P every half-cycle. Because the current variation is so large, the power supply used in a push-pull amplifier must be particularly well regulated-that is, it must maintain a constant voltage, independent of current demand.

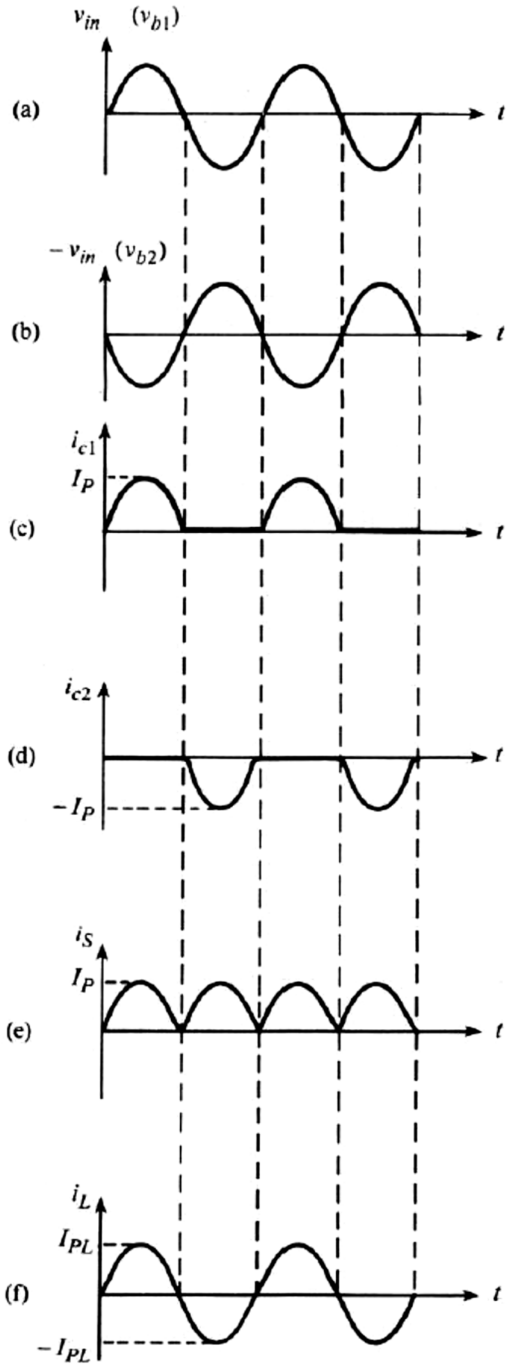


Fig. 3-12

3.4.3 Class-B Efficiency:

The principal advantage of using a class-B power amplifier is that it is possible to achieve an efficiency greater than that attainable in a class-A amplifier. The improvement in efficiency stems from the fact that no power is dissipated in a transistor during the time intervals that it is cut off. Also, like the transformer-coupled class-A amplifier, there is no external collector resistance that would otherwise consume power.

We will derive an expression for the maximum efficiency of a class-B push-pull power amplifier assuming ideal conditions: perfectly matched transistors and zero resistance in the transformer windings. The current supplied by each transistor is a

half-wave-rectified waveform, as shown in Fig. 3-12. Let I_P represent the peak value of each. Then the peak value of the current in the secondary winding, which is the same as the peak load current, is

$$I_{PL} = (N_p/N_s)I_P$$

where N_p/N_s, is the turns ratio between one-half the primary winding and the secondary winding ($N_p = N_{p(\text{total})}/2$). Note that only those primary turns between one end of the winding and its center tap are used to induce current in the secondary. Similarly, the peak value of the load voltage is

$$V_{PL} = (N_s/N_p)V_P$$

where V_P is the peak value of the primary (collector) voltage. Since the load voltage and load current are sinusoidal, the average power delivered to the load is, from Eqn. [3-4],

$$P_L = \frac{V_{PL}I_{PL}}{2} = \frac{(N_s/N_p)V_P(N_p/N_s)I_P}{2} = \frac{V_P I_P}{2}.$$

As shown in Fig. 3-12(e), the power-supply current is a full-wave-rectified waveform having peak value I_P. The dc, or average, value of such a waveform is known to be $2I_p/\pi$. Therefore, the average power delivered to the circuit by the dc supply is

$$P_S = \frac{2I_P V_{CC}}{\pi}.$$

The efficiency is then

$$\eta = \frac{P_L}{P_S} = \frac{V_P I_P/2}{2I_P V_{CC}/\pi} = \frac{\pi V_P}{4V_{CC}} \qquad [3\text{-}12]$$

Under maximum signal conditions, $V_P = V_{CC}$, and Eqn. [3-12] becomes

$$\eta(\text{max}) = \frac{\pi}{4} = 0.785$$

This equation shows that a class-B push-pull amplifier can be operated with a much higher efficiency than the class-A amplifiers studied earlier. Furthermore, unlike the case of class-A amplifiers, the power dissipated in the transistors is 0 under standby (zero signal) conditions, because both transistors are cut off. A general expression for the total power dissipated in the transistors can be obtained by realizing that it equals the difference between the total power supplied by the dc source and the total power delivered to the load:

$$P_d = P_S - P_L = \frac{2I_P V_{CC}}{\pi} - \frac{V_P I_P}{2}.$$

Using calculus, it can be shown that P_d is maximum when $V_P = 2V_{CC}/\pi = 0.636V_{CC}$. We conclude that maximum transistor dissipation does not occur when maximum load power is delivered ($V_P = V_{CC}$), but at the intermediate level $V_P = 0.636V_{CC}$.

Exercise 3-4:

The push-pull amplifier in Fig. 3-10 has V_{CC} = 20 V and R_L = 10 Ω. The total number of turns on the primary winding is 100 and the secondary winding has 50 turns. Assume that the transformer has zero resistance.

(a) Find the maximum power that can be delivered to the load.
(b) Find the power dissipated in each transistor when maximum power is delivered to the load.
(c) Find the power delivered to the load and the power dissipated in each transistor when transistor power dissipation is maximum.

[Answers: (a) 20 W, (b) 2.73 W, (c) 8.09 W, 4.05 W]

3.4.4 Push-Pull Drivers:

The push-pull amplifier must be driven by out-of-phase input signals. Fig. 3-13 shows how a transformer can be used to provide the required drive signals. Here, the secondary winding has a grounded center tap that effectively splits the secondary voltage into two out-of-phase signals, each having one-half the peak value of the total secondary voltage. The input signal is applied across the primary winding and a voltage is developed across secondary terminals A-B, in the usual transformer fashion.

To understand the phase splitting action, consider the instant at which the voltage across A-B is +6 V, as shown in the figure. Then, since the center point is at ground, the voltage from A to ground must be +3 V and that from B to ground must be −3V:

$V_{AB} = V_A - V_B = 3 - (-3) = +6$ V.

The same logic applied at every instant throughout a complete cycle shows that v_B with respect to ground is always the negative of v_A with respect to ground; in other words, v_A and v_B are equal-amplitude, out-of-phase driver signals, as required.

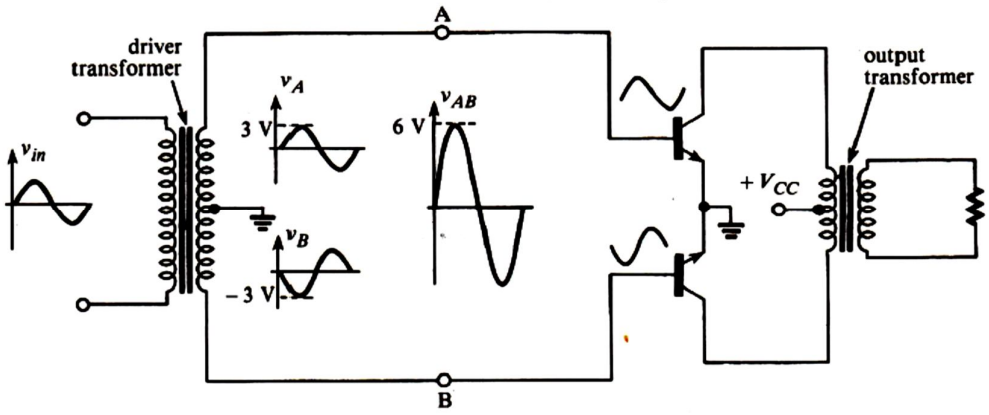
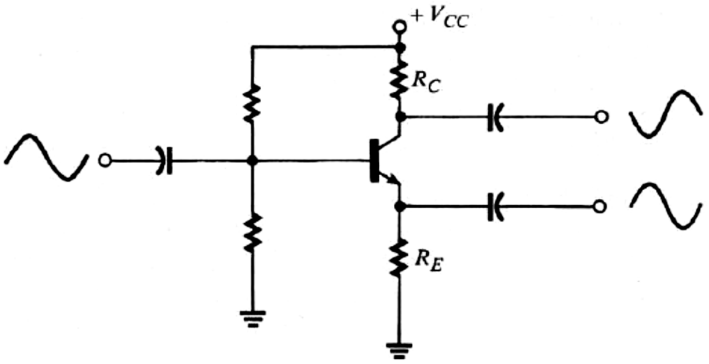


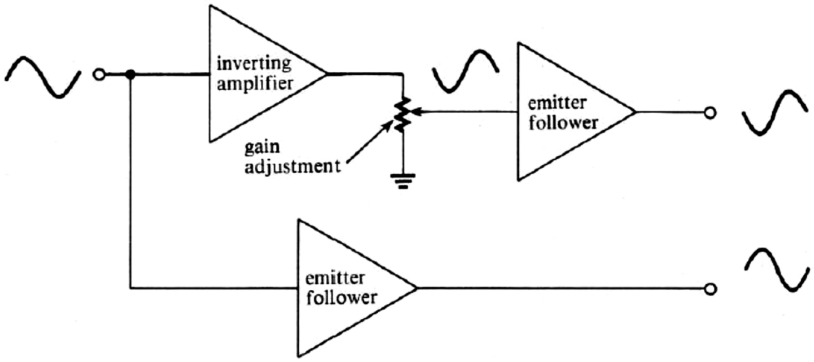
Fig. 3-13

A specially designed amplifier, called a phase-splitter, can be used instead of a driver transformer to produce equal-amplitude, out-of-phase drive signals. Fig. 3-14 shows two possible designs. Fig. 3-13(a) is a conventional amplifier circuit with outputs taken at the collector and at the emitter. The collector output is out of phase with the input and the emitter output is in phase with the input, so the two outputs are out of phase with each other. With no load connected to either output, the output signals will have approximately equal amplitudes if $R_C = R_E$. However, the output impedance at the collector is significantly greater than that at the emitter, so when loads are connected, each output will be affected differently.

As a consequence, the signal amplitudes will no longer be equal, and gain adjustments will be required. Furthermore, the nonlinear nature of the large signal load (the output transistors) means that the gain of the collector output may vary appreciably with signal level. Intolerable distortion can be created as a result. A better way to drive the output transistors is from two low-impedance signal sources, as shown in Fig. 3-14(b). Here, the output from an inverting amplifier is buffered by an emitter-follower stage, as is the original signal.



(a)



(b)

Fig. 3-14

3.4.5 Distortion in Push-Pull Amplifiers:

***Cancellation of Even Harmonics*:**

Recall that push-pull operation effectively produces in a load a waveform proportional to the difference between two input signals. Under normal operation, the signals are out of phase, so their waveform is reproduced in the load. If the signals were in phase, cancellation would occur. It can be shown that a half-wave-rectified sine wave contains only the fundamental and all even harmonics. Fig. 3-15(a) shows the two out-of-phase half-wave-rectified sine waves that drive the load, and Fig. 3-15(b) shows the fundamental and second-harmonic components of each. The fundamental components are out of phase. Therefore, the fundamental component is reproduced in the load, as we have already seen (Fig. 3-12). However, the second-harmonic components are in phase, and therefore cancel in the load. Although not shown in Fig. 3-15(b), the fourth and all other even harmonics are also in phase and therefore also cancel. Our conclusion is an important property of push-pull amplifies: even harmonics are cancelled in push-pull operation.

The cancellation of even harmonics is an important factor in reducing distortion in push-pull amplifiers. However, perfect cancellation would occur only if the two sides were perfectly matched and perfectly balanced: identical transistors, identical drivers, and a perfectly center-tapped transformer. Of course, this is not the case in practice, but even imperfect push-pull operation reduces even harmonic distortion. Odd harmonics are out of phase, so cancellation of those components does not occur.

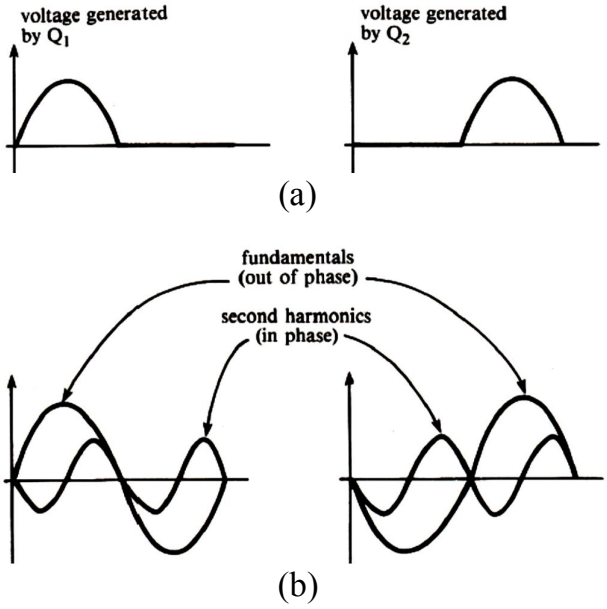


Fig. 3-15

Crossover Distortion:

A forward-biasing voltage applied across a PN junction must be raised to a certain level (about 0.7 V for silicon) before the junction will conduct any significant current. Similarly, the voltage across the base-emitter junction of a transistor must reach that level before any appreciable base current, and hence collector current, can flow. As a consequence, the drive signal applied to a class-B transistor must reach a certain minimum level before its collector current is properly in the active region. This fact is the principal source of distortion in a class-B, push-pull amplifier, as illustrated in Fig. 3-16.

Fig. 3-16(a) shows that the initial rise of collector current in a class-B transistor lags the initial rise of input voltage, for the reason we have described. Also, collector current prematurely drops to 0 when the input voltage approaches 0. Fig. 3-16(b) shows the voltage wave form that is produced in the load of a push-pull amplifier when the distortion generated during each half-cycle by each class-B transistor is combined. This distortion is called ***crossover distortion***, because it occurs where the composite waveform crosses the zero voltage axes. Clearly, the effect of crossover distortion becomes more serious as the signal level becomes smaller.

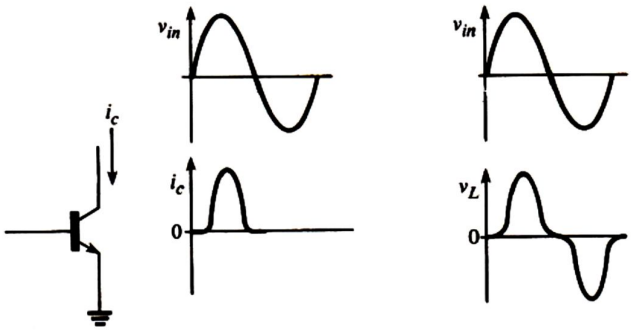
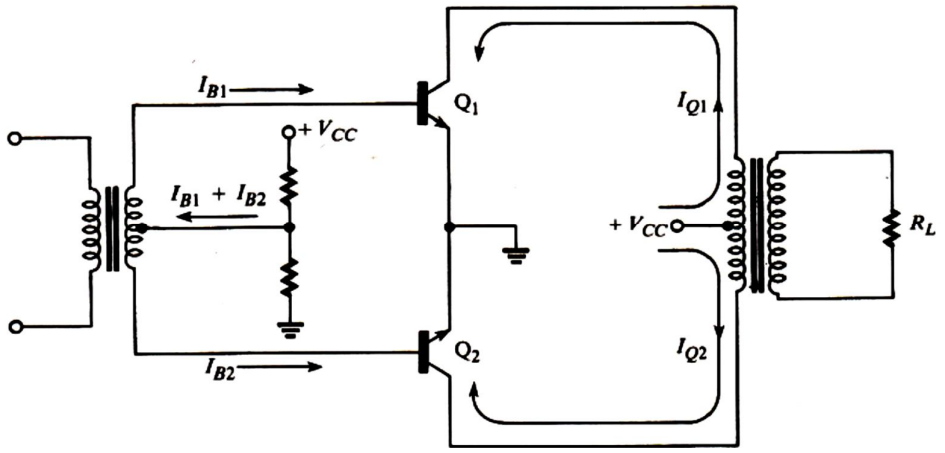


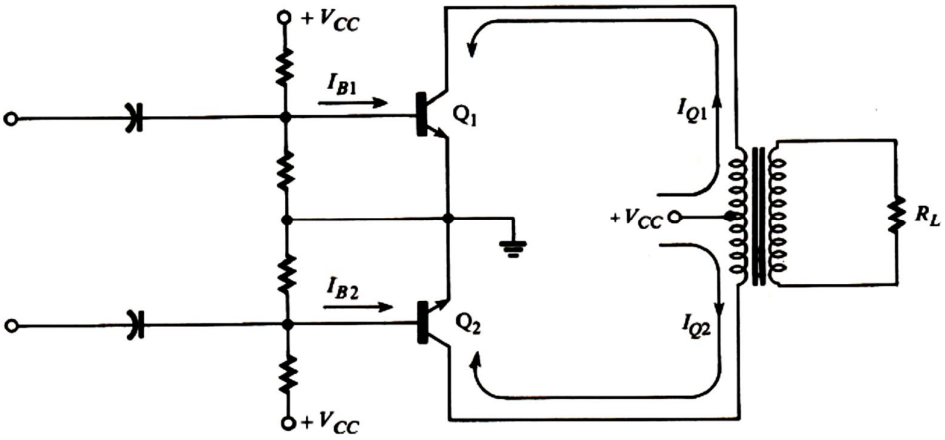
Fig. 3-16

2.5 Class-AB Power Amplifiers:

Crossover distortion can be reduced or eliminated in a push-pull amplifier by biasing each transistor slightly into conduction. When a small forward-biasing voltage is applied across each base-emitter junction, and a small base current flows under no-signal conditions, it is not necessary for the base drive signal to overcome the built-in junction potential before active operation can occur. A simple voltage-divider bias network can be connected across each base for this purpose, as shown in Fig. 3-17. Fig. 3-17(a) shows how two resistors can provide bias for both transistors when a driver transformer is used. Fig. 3-17(b) shows the use of two voltage dividers when the drive signals are capacitor coupled. Typically, the base-emitter junctions are biased at about 0.5 V for silicon transistors, or so that the collector current under no-signal conditions is about 1% of its peak signal value.



(a)



(b)

Fig. 3-17

When a transistor is biased slightly into conduction, output current will flow during more than one-half cycle of a sine-wave input, as illustrated in Fig. 3-18. As can be seen in the figure, conduction occurs for more than one-half but less than a full cycle of input. This operation, which is neither class A nor class B, is called class-AB operation.

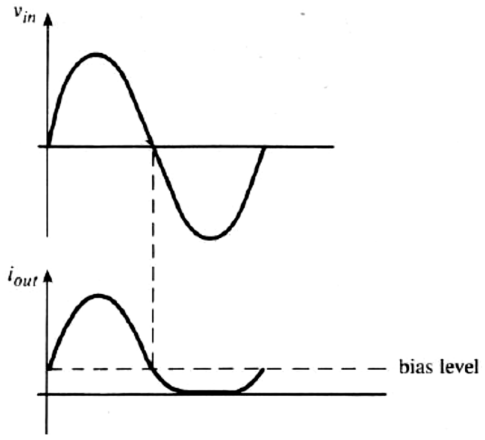


Fig. 3-18

While class-AB operation reduces crossover distortion in a push-pull amplifier, it has the disadvantage of reducing amplifier efficiency. The fact that bias current is always present means that there is continuous power dissipation in both transistors, including the time intervals during which one of the transistors would be cut off if the operation were class B. The extent to which efficiency is reduced depends directly on how heavily the transistors are biased, and the maximum achievable efficiency is somewhere between that which can be obtained in class-A operation (0.5) and that attainable in class-B operation (0.785).

In Fig. 3-17, the quiescent collector currents I_{Q1} and I_{Q2} flow in opposite directions though the primary of the transformer. Thus, the magnetic flux created in the transformer by one dc current opposes that created by the other, and the net flux is 0. This is an advantageous situation, in comparison with the class-A transformer-coupled amplifier, because it means that transformer current can swing positive and negative through a maximum range. If the transformer flux had a bias component, the signal swing would be limited in one direction by the onset of magnetic saturation.

3.6 Transformerless Push-Pull Amplifiers:

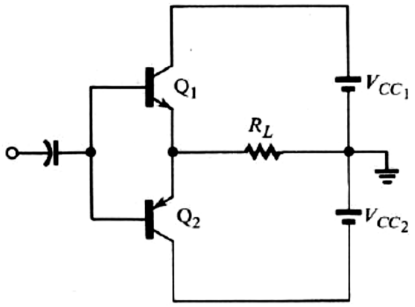
The principal disadvantage of the push-pull amplifier circuits we have discussed so far is the cost and bulk of their output transformers. High-power amplifiers in particular are encumbered by the need for very large transformers capable of conducting large currents without saturating.

3.6.1 Complementary Push-Pull Amplifiers:

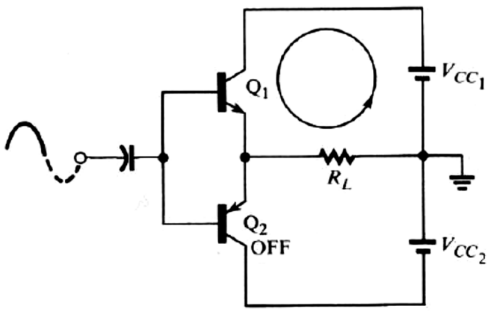
Fig. 3-19(a) shows a popular design using complementary (PNP and NPN) output transistors to eliminate the need for an output transformer in push-pull operation. This design also eliminates the need for a driver transformer or any other drive circuitry producing out-of-phase signals.

Fig. 3-19(b) shows that current flows in a counterclockwise path through the load when the input signal on the base of NPN transistor Q_1 is positive. The positive inputs, simultaneously, appears on the base of PNP transistor Q_2 and keeps it cut off. When the input is negative, Q_1 is cut off and Q_2 conducts current through the load in the opposite direction, as shown in Fig. 3-19(c).

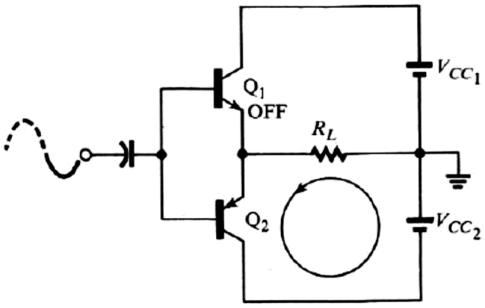
Each transistor in Fig. 3-19 drives the load in an emitter-follower configuration. The advantageous consequence is that low-impedance loads can be driven from a low impedance source. Also, the large negative feedback that is inherent in emitter-follower operation reduces the problem of output distortion. However, as is the case in all emitter followers, voltage gains greater than unity cannot be realized. The maximum positive voltage swing is V_{CC1} and the maximum negative swing is V_{CC2}. Normally, $|V_{CC1}| = |V_{CC2}| = |V_{CC}|$, so the maximum peak-to-peak swing is $2V_{CC}$ volts. Since the voltage gain is near unity, the input must also swing through $2V_{CC}$ volts to realize maximum output swing. Under conditions of maximum swing, the cut-off transistor has a reverie-biasing collector-to-base voltage of $2V_{CC}$ volts, so each transistor must have a rated breakdown voltage of at least that amount.



(a)



(b)

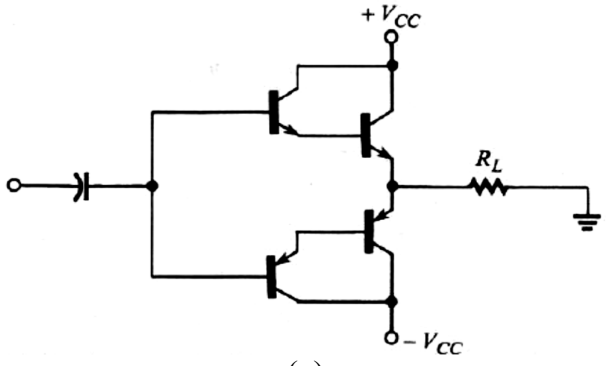


(c)

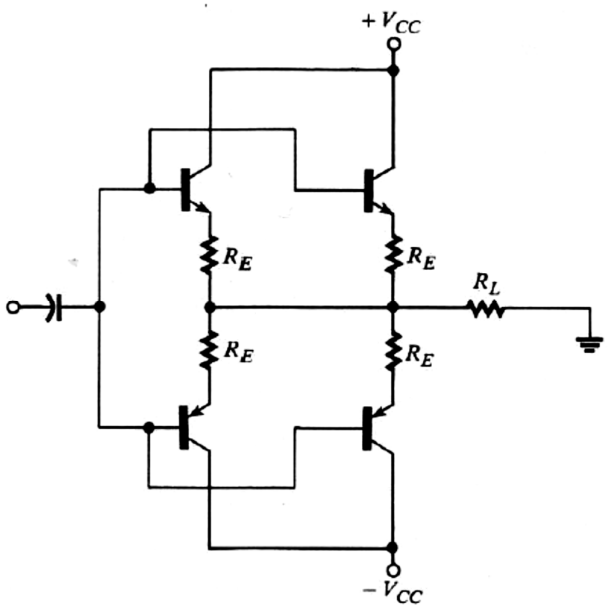
Fig. 3-19

Fig. 3.20 shows two variations on the basic complementary, push-pull amplifier. In Fig. 3.20(a), the transistors are replaced by emitter-follower Darlington pairs. Since power transistors tend to have low betas, particularly at high current levels, the Darlington pair improves the drive capabilities and the current gain of the amplifier. These devices are available in matched complementary sets with current ratings up to 20 amperes.

Fig. 3-20(b) shows how emitter-follower transistors can be operated in parallel to increase the overall current-handling capability of the amplifier. In this variation, the parallel transistors must be closely matched to prevent "current hogging", wherein one device carries most of the load, thus subverting the intention of load sharing. Small emitter resistors R_E shown in the figure introduce negative feedback and help prevent current hogging, at the expense of efficiency. Amplifiers capable of dissipating several hundred watts have been constructed using this arrangement.



(a)



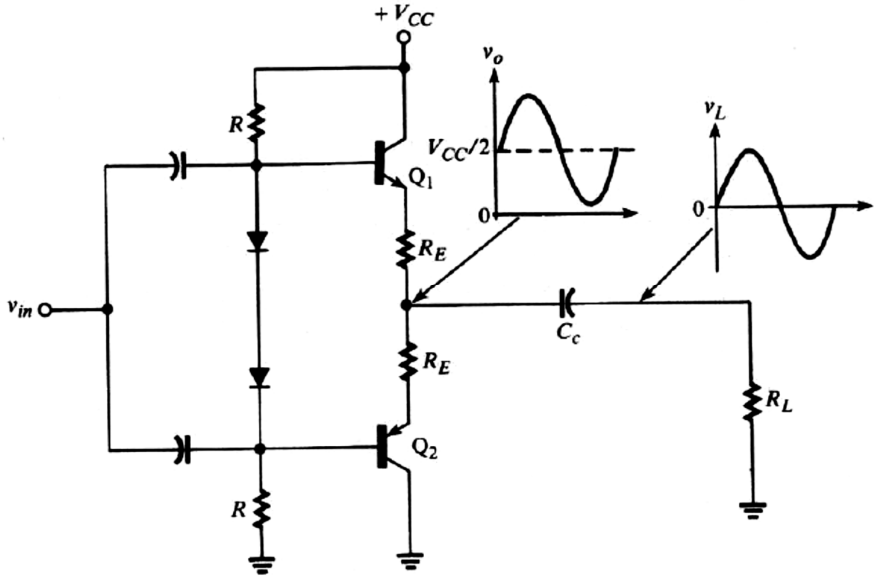
(b)

Fig. 3-20

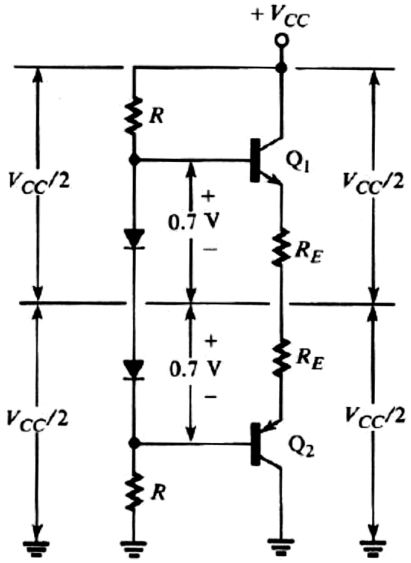
One disadvantage of the complementary push-pull amplifier is the need for two power supplies. Also, like the transformer-coupled push-pull amplifier, the complementary class-B amplifier produces crossover distortion in its output. Fig. 3-21(a) shows another version of the complementary amplifier that eliminates these problems and that incorporates some additional features.

The complementary amplifier in Fig. 3-21 can be operated with a single power supply because the output v_o, is biased at half the supply voltage and is capacitor-coupled to the load. The resistor-diode network connected across the transistor bases is used to bias each transistor near the threshold of conduction. Crossover distortion can be reduced or eliminated by inserting another resistor (not shown in the figure) in series with the diodes to bias the transistors further into AB-operation. Assuming that an components are perfectly matched, the supply voltage will divide equally across each half of the amplifier, as shown in Fig. 3.21(b). In practice, one of the resistors R can be made adjustable for balance purposes. Resistors R_E provide bias stability to prevent thermal runaway, but are made as small as possible since they adversely affect efficiency. Since each half of the

amplifier has $V_{CC}/2$ volts across it, the forward-biased diode drops appear across the base-emitter junctions with the proper polarity to bias each transistor towards conduction. The diodes are selected so that their characteristics track the base emitter junctions under temperature changes and thus ensure bias stability. The diodes are typically mounted on the same heat sinks as the transistors so that both change temperature in the same way.



(a)



(b)

Fig. 3-21

In ac operation, when input v_1 is positive and Q_1 is conducting, current is drawn from the power supply and flows through Q_1 to the load. When Q_1 is cut off by a negative input, no current can flow from the supply. At those times, Q_2 is conducting and capacitor C_c discharges through that transistor. Thus, current flows from the load through C_c, and through Q_2 to ground whenever the input is negative.

The R_LC_c time constant must be much greater than the period of the lowest signal frequency. The lower cutoff frequency due to C_c is given by

$$f_L(C_c) = \frac{1}{2\pi(R_L+R_E)C_c} \quad [3\text{-}13]$$

The peak load current is the peak input voltage V_P divided by $R_L + R_E$:

$$I_{PL} = \frac{V_P}{R_L+R_E}$$

Therefore, the average ac power delivered to the load is

$$P_L = \frac{I_{PL}^2 R_L}{2} = \frac{V_P^2 R_L}{2(R_L+R_E)^2}$$

Since current is drawn from the power supply only during positive half-cycles of input, the supply-current waveform is half-wave rectified, with peak value $V_P/(R_L + R_E)$ amperes. Therefore, the average value of the supply current is

$$I_S(\text{avg}) = \frac{V_P}{\pi(R_L+R_E)}$$

and the average power from the supply is

$$P_S = V_{CC} I_S(\text{avg}) = \frac{V_{CC}V_P}{\pi(R_L+R_E)}$$

We find the efficiency to be

$$\eta = \frac{P_L}{P_S} = \frac{\pi}{2}\left(\frac{R_L}{R_L+R_E}\right)\left(\frac{V_P}{V_{CC}}\right) \quad [3\text{-}14]$$

The efficiency is maximum when the peak voltage V_P has its maximum possible value, $V_{CC}/2$. In that case,

$$\eta(\text{max}) = \frac{\pi}{2}\left(\frac{R_L}{R_L+R_E}\right)\left(\frac{V_{CC}/2}{V_{CC}}\right) = \frac{\pi}{4}\left(\frac{R_L}{R_L+R_E}\right)$$

The last two equations show that efficiency decreases, as expected, when R_E is increased. If R_E = 0, then the maximum possible efficiency becomes $\eta(\text{max}) = \pi/4 = 0.785$, the theoretical maximum for a class-B amplifier.

3.6.2 Quasi-Complementary Push-Pull Amplifiers:

Modern semiconductor technology is such that NPN transistors are generally superior to PNP types. Fig. 3-22 shows a popular push-pull amplifier design that uses NPN transistors for both output devices. This design is called quasi-complementary because transistors Q_3 and Q_4 together perform the same function as the PNP transistor in a complementary push-pull amplifier.

When the input signal is positive, PNP transistor Q_3 is cut off, so NPN transistor Q_4 receives no base current and is also cut off. When the input is negative, Q_3 conducts and supplies base current to Q_4, which can then conduct load current. Transistors Q_1 and Q_2, form an NPN Darlington pair, so Q_1 and Q_2 provide emitter-follower action to the load when the input is positive, and Q_3 and Q_4 perform that function when the input is negative. The entire configuration thus performs push-pull operation in the same manner as the complementary push-pull amplifier. The current gain of the Q_3Q_4 combination is

$$\frac{I_E}{I_B} = \beta_3\beta_4 + (1 + \beta_3)$$

This gain is very nearly that of a Darlington pair. Transistors Q_1 and Q_2 are connected as a Darlington pair to ensure that both sides of the amplifier have similar gain.

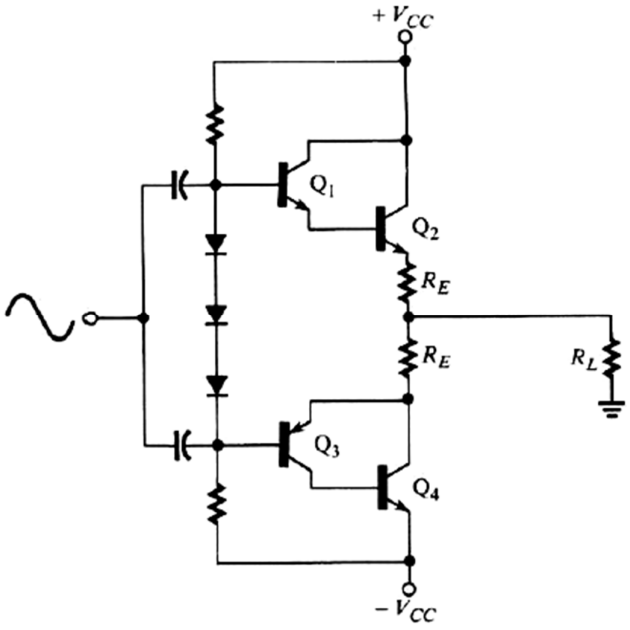


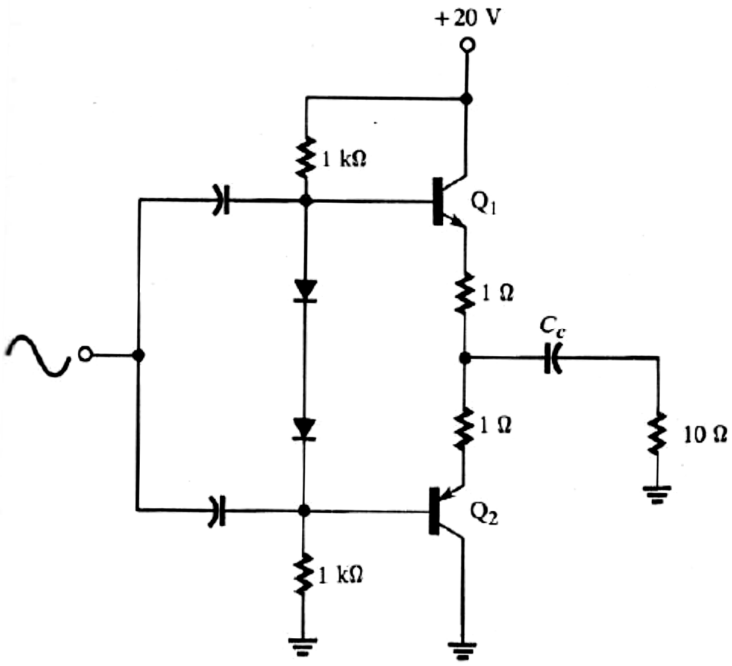
Fig. 3-22

Exercise 3-5:

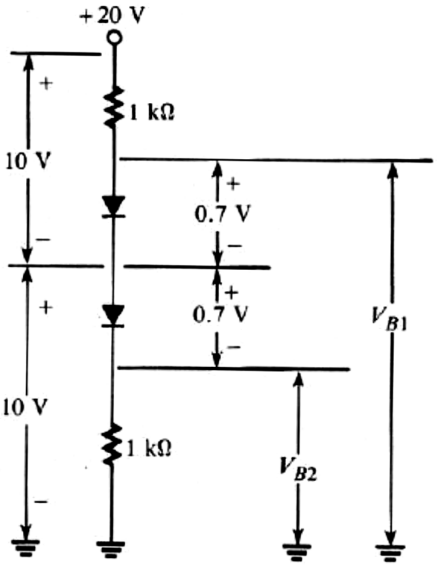
Assuming that all components in Fig. 3-23(a) are perfectly matched, find

(a) the base-to-ground voltages V_{B1} and V_{B2} of each transistor,
(b) the power delivered to the load under maximum signal conditions,
(c) the efficiency under maximum signal conditions, and
(d) the value of capacitor C_c if the amplifier is to be used at signal frequencies down to 20 Hz.

[Answers: (a) 10.7 V, 9.3 V, Fig. 3-23(b), (b) 4.132 W, (c) 0.714, (d) 723 μF]



(a)



(b)

Fig. 3-23

3.7 Class-C Power Amplifiers:

A class-C amplifier is one whose output conducts load current during less than one-half cycle of an input sine wave. Fig. 3-24 shows a typical class-C current waveform, and it is apparent that the total angle during which current flows-is less than 180º. This angle is called the conduction angle, θ_c.

Of course, the output of a class-C amplifier is a highly distorted version of its input. It could not be used in an application requiring high fidelity, such as an audio amplifier. Class-C amplifiers are used primarily in high-power, high-frequency applications, such as radio-frequency transmitters. In these applications, the high-frequency pulses handled by the amplifier are not themselves the signal, but constitute what is called the carrier for the signal. The signal is transmitted by varying the amplitude of the carrier, using the process called, amplitude modulation (AM). The signal is ultimately recovered in a receiver by filtering out the carrier frequency. The principal advantage of a class-C amplifier is that it has a very high efficiency.

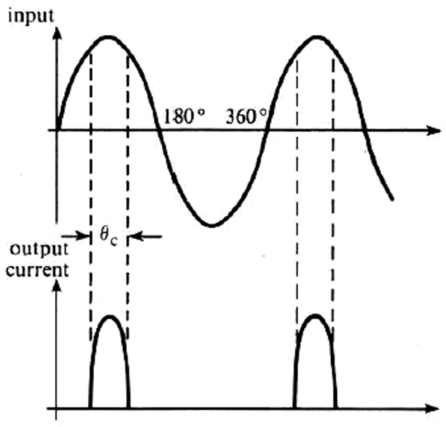


Fig. 3-24

Fig. 3-25 shows a simple class-C amplifier with a resistive load. The base of the NPN transistor is biased by a negative voltage, $-V_{BB}$, connected through a coil labeled RFC. The RFC is a radio-frequency choke whose inductance presents a high impedance to the high-frequency input and thereby prevents the dc source from shorting the ac input. In order for the transistor to begin conducting, the input must reach a level sufficient to overcome both the negative bias and the V_{BE} drop of about 0.7 V:

$$V_c = |V_{BB}| + 0.7$$

where V_c is the input voltage at which the transistor begins to conduct. As shown in the figure, the transistor is cut off until v_{in} reaches V_c, then it conducts, and then it cuts off again when v_{in} falls below V_c. Clearly, the more negative the value of V_{BB}, the shorter the conduction interval. In most class-C applications, the amplifier is designed so that the peak value of the input, V_P, is just sufficient to drive the transistor into saturation.

The conduction angle θ_c in Fig. 3-25 can be found from

$$\theta_c = 2 \arccos\left(\frac{V_c}{V_P}\right)$$

where V_P is the peak input voltage that drives the transistor to saturation. If the peak input only just reaches V_c, then $\theta_c = 2 \arccos(1) = 0º$. At the other extreme, if $V_{BB} = 0$, then $V_c = 0.7$, $(V_c/V_P) \approx 0$, and $\theta_c = 2 \arccos(0) = 180$ °, which corresponds to class-B operation.

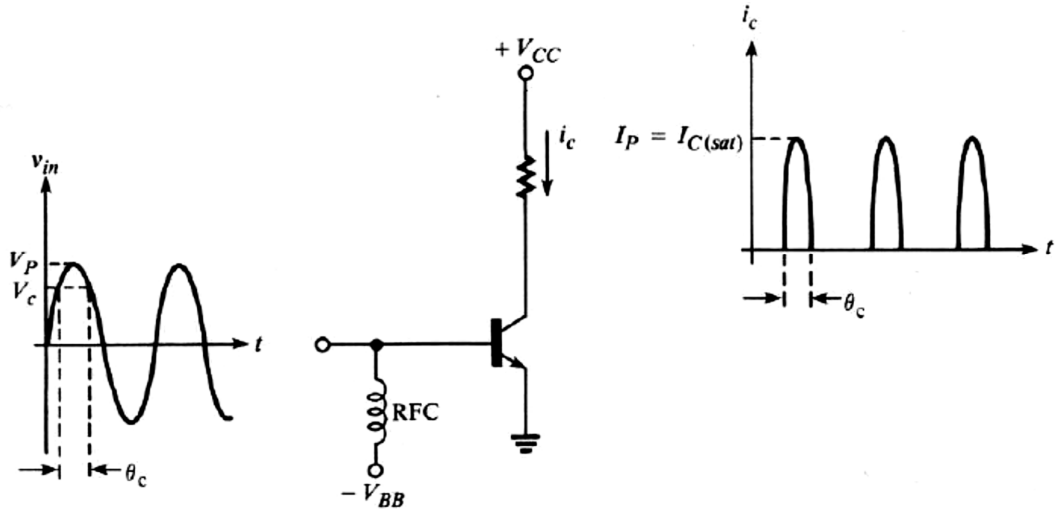


Fig. 3-25

Fig. 3-26 shows the class-C amplifier as it is normally operated, with an LC tank network in the collector circuit. The tank is a resonant network whose center frequency, assuming small coil resistance, is closely approximated by

$$f_o \approx \frac{1}{2\pi\sqrt{LC}}$$

The purpose of the tank is to produce the fundamental component of the pulsed, class-C waveform, which has the same frequency as v_{in}. The configuration is called a tuned amplifier, and the center frequency of the tank is set equal to (tuned to) the input frequency. There are several ways to view its behavior as an aid in understanding how it recovers the fundamental frequency. We may regard the tank as a highly selective (high-Q) filter that suppresses the harmonics in the class-C waveform and passes its fundamental. The voltage gain of the transistor equals the impedance in the collector circuit divided by the emitter resistance. Since the impedance of the tank is very large at its center frequency, the gain is correspondingly large at that frequency, while the impedance and the gain at harmonic frequencies are much smaller.

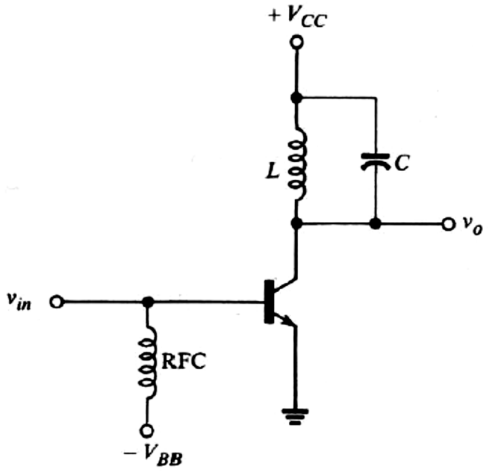


Fig. 3-26

The amplitude of the fundamental component of a class-C waveform depends on the conduction angle θ_c. The greater the conduction angle, the greater the ratio of the amplitude of the fundamental component to the amplitude of the total waveform. Let r_1 be the ratio of the peak value of the fundamental component to the peak value of the class-C waveform. The value of r_1 is closely approximated by

$$r_1 \approx (-3.54 + 4.1\,\theta_c - 0.0072\,\theta_c^2) \times 10^{-3}$$

where $0^\circ \le \theta_c \le 180^\circ$. The values of r_1 vary from 0 to 0.5 as θ_c varies from 0º to 180º.

Let r_0 be the ratio of the dc value of the class-C waveform to its peak value. The value of r_0 can be found from

$$r_0 = \frac{\text{dc value}}{\text{peak value}} = \frac{\theta_c}{\pi(180)}$$

where $0^\circ \le \theta_c \le 180^\circ$. The values of r_0 vary from 0 to $1/\pi$ as θ_c varies from 0º to 180º.

The efficiency of a class-C amplifier is large because very little power is dissipated when the transistor is cut off, and it is cut off during most of every full cycle of input. The output power at the fundamental frequency under maximum drive conditions is

$$P_o = \frac{(r_1 I_P)V_{CC}}{2}$$

where I_P is the peak output (collector) current. The average power supplied by the dc source is V_{CC} times the average current drawn from the source. Since current flows only when the transistor is co ducting, this current waveform is the same as the class-C collector-current waveform having peak value I_P. Therefore,

$$P_S = (r_0 I_P)V_{CC}$$

The efficiency is then

$$\eta_c = \frac{P_o}{P_S} = \frac{r_1 I_P V_{CC}}{2 r_0 I_P V_{CC}} = \frac{r_1}{2 r_0} \qquad [3\text{-}15]$$

Exercise 3-6:

A class-C amplifier has a base bias voltage of −5 V and V_{CC} = 30 V. It is determined that a peak input voltage of 9.8 V at 1 MHz is required to drive the transistor to its saturation current of 1.8 A.

(a) Find the conduction angle.
(b) Find the output power at 1 MHz.
(c) Find the efficiency.
(d) If an LC tank having C = 200pF is connected in the collector circuit, find the inductance necessary to tune the amplifier.

[Answers: (a) 108.9º, (b) 9.64 W, (c) 0.925, (d) 0.127 mH]

Oscillators

4.1 General Concepts:

An ***oscillator*** is a device that generates a periodic ac output signal without any form of input signal required with only the dc supply voltage as an input. The output voltage can be either ***sinusoidal*** or ***nonsinusoidal*** (see Fig. 4-1). Two major classifications of oscillators are ***feedback*** oscillators and ***relaxation*** oscillators; an oscillator is designed to have a feedback path with known characteristics, so that a predictable oscillation will occur at a predetermined frequency.

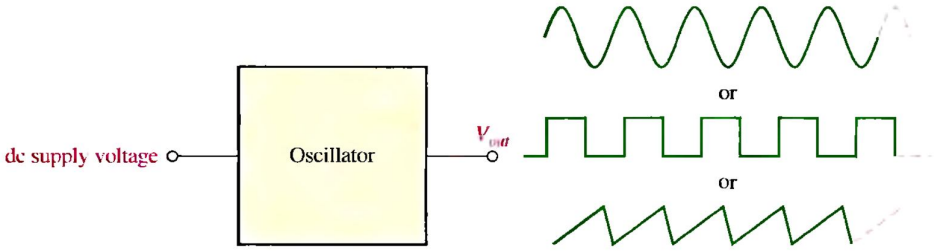


Fig. 4-1

One type of oscillator is the feedback oscillator, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal. After oscillations are started, the loop gain is maintained at 1 to maintain oscillations. A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp) and a positive feedback circuit that produces phase shift and provides attenuation, as shown in Fig. 4-2.

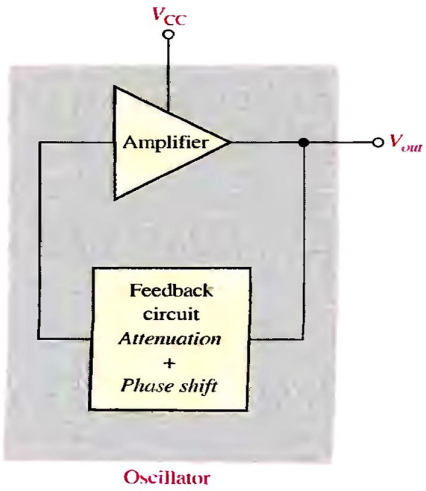


Fig. 4-2

A second type is a relaxation oscillator uses an *RC* timing circuit to generate a waveform that is generally a square wave or other nonsinusoidal waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

4.2 Feedback Oscillators:

Feedback oscillator operation is based on the principle of positive feedback. Feedback oscillators are widely used to generate sinusoidal waveforms. Positive feedback is characterized by the condition wherein an in-phase portion of the output voltage of an amplifier is fed back to the input with no net phase shift, resulting in a reinforcement of the output signal. As shown in Fig. 4-3, the in-phase feedback voltage, V_f is amplified to produce the output voltage, which in turn produces the feedback voltage. That is, a loop is created in which the signal sustains itself and a continuous sinusoidal output is produced. This phenomenon is called ***oscillation***.

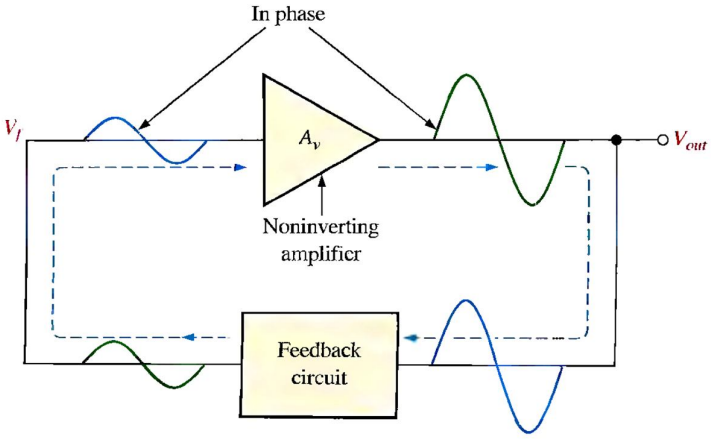


Fig. 4-3

Two conditions, illustrated in Fig. 4-4, are required for a sustained state of oscillation:

1. The phase shift around the feedback loop must be effectively 0°.

2. The voltage gain, A, around the closed feedback loop (loop gain) must equal 1 (unity).

The unity-gain condition must be met for oscillation to be sustained. For oscillation to begin, the voltage gain around the positive feedback loop must be greater than 1 so that the amplitude of the output can build up to a desired level. The gain must then decrease to 1 so that the output stays at the desired level and oscillation is sustained.

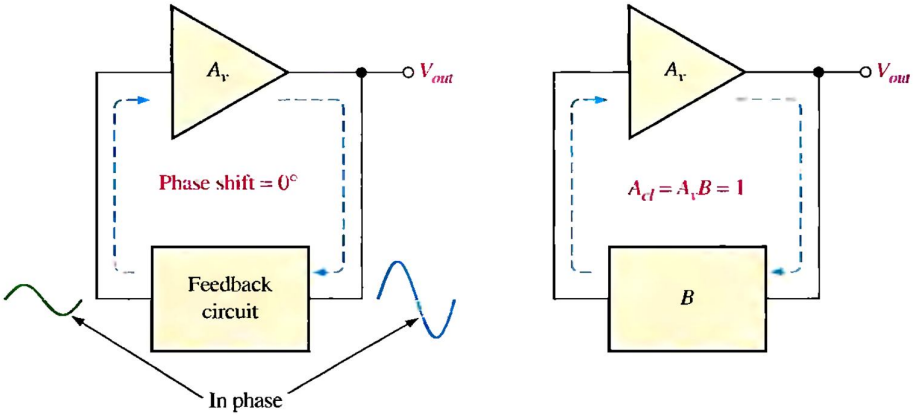


Fig. 4-4

A question that normally arises is this: If the oscillator is initially off and there is no output voltage. How does a feedback signal originate to start the positive feedback buildup process? Initially a small positive feedback voltage develops from thermally produced broad-band noise in the resistors or other components or from power supply turn-on transients. The feedback circuit permits only a voltage with a frequency equal to the selected oscillation frequency to appear in phase on the amplifier's input. This initial feedback voltage is amplified and continually reinforced, resulting in a buildup of the output voltage, as illustrated in Fig. 4-5.

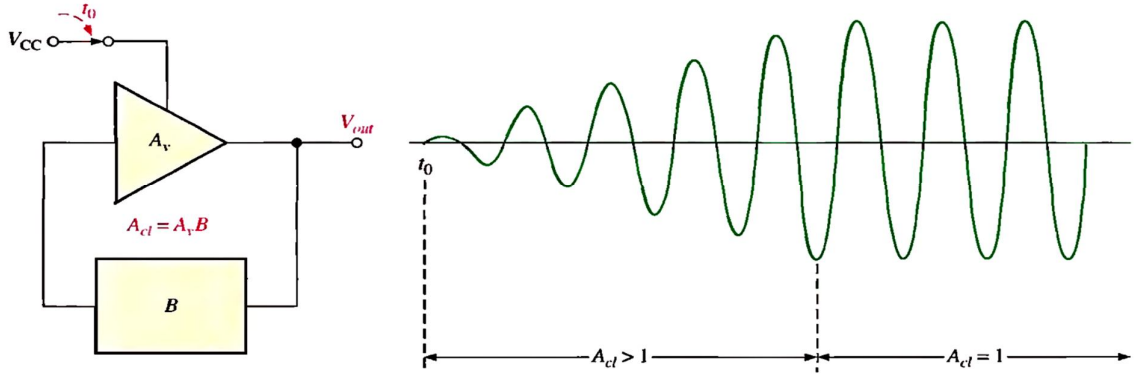


Fig. 4-5

Finally, what we mean by "feedback" feedback to where? In reality, it makes no difference where, because we have a closed loop with no summing junction at which any external input is added (see Fig. 4-5). Thus, we could start anywhere in the loop and call that point both the "input" and the "output"; we could think of the "feedback" path as the entire path through which signal flows in going completely around the loop of an amplifier having gain A and a feedback path having gain B. Every oscillator must have an amplifier, or equivalent device, in order for the system oscillate, the loop gain AB must satisfy the ***Barkhausen criterion***, namely, $AB = 1$. The unity loop-gain criterion for oscillation is often called positive feedback. To understand and apply the Barkhausen criterion, we must regard both the gain and the phase shift of AB as functions of frequency. To show the dependence of the loop gain AB on frequency, we write $AB(j\omega)$, a complex phasor that can be expressed in both polar and rectangular form:

$$AB(j\omega) = |AB|\angle\theta = |AB|cos\,\theta + j|AB|\sin\theta$$

where $|AB|$ is the gain magnitude, a function of frequency, and θ is the phase shift, also a function of frequency. The Barkhausen criterion requires that:

$$|AB| = 1 \quad \text{and} \quad \theta = \pm 360°n$$

where n is any integer, including 0. In polar and rectangular forms, the Barkhausen criterion is expressed as:

$$AB(j\omega) = 1\angle \pm 360°n = 1 + j0$$

4.3 Oscillators with RC Feedback Circuits:

In this section, we will study two types of feedback oscillators that use RC circuits to produce sinusoidal outputs: the Wien-bridge oscillator and the phase-shift oscillator. Generally, RC feedback oscillators are used for frequencies up to about 1 MHz.

4.3.1 Wien-Bridge Oscillators:

One type of sinusoidal feedback oscillator is the ***Wien-bridge*** oscillator. A fundamental part of the Wien-bridge oscillator is a lead-lag circuit like that shown in Fig. 4-6(a). R_1 and C_1 together form the lag portion (LPF) of the circuit; R_2 and C_2 form the lead portion (HPF). The operation of this lead-lag (BPF) circuit is as follows. At lower frequencies, the lead circuit dominates due to the high reactance of C_2. As the frequency increases, X_{C2} decreases, thus allowing the output voltage to increase. At some specified frequency, the response of the lag circuit takes over, and the decreasing value of X_{C1} causes the output voltage to decrease.

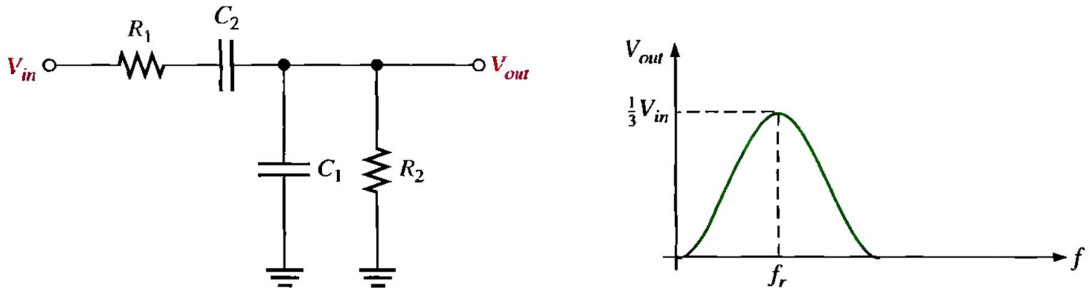
The response curve for the lead-lag circuit shown in Fig. 4-6(b) indicates that the output voltage peaks at a frequency called the resonant frequency, f_r. At this point the attenuation (V_{out}/V_{in}) of the circuit is 1/3 if $R_1 = R_2 = R$ and $C_1 = C_2 = C$ as stated by the following equation:

$$B = \frac{V_{out}}{V_{in}} = \frac{1}{3} \qquad [4\text{-}1]$$

The formula for the resonant frequency is

$$f_r = \frac{1}{2\pi RC} \qquad [4\text{-}2]$$

To summarize, the lead-lag circuit in the Wien-bridge oscillator has a resonant frequency, f_r, at which the phase shift through the circuit is 0° and the attenuation is 1/3. Below f_r, the lead circuit dominates and the output leads the input. Above f_r, the lag circuit dominates and the output lags the input.



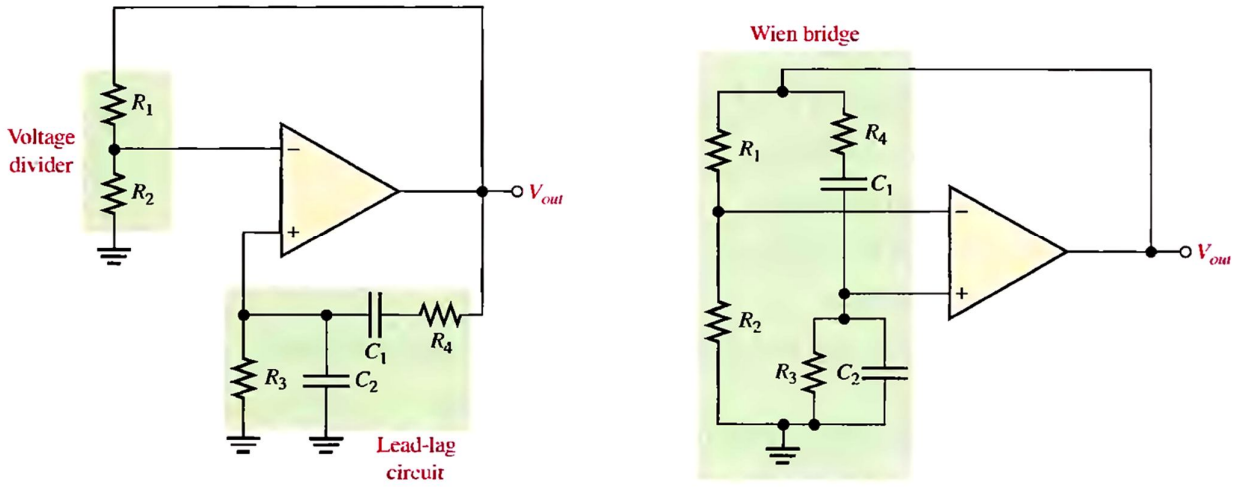
(a) (b)

Fig. 4-6

The lead-lag circuit is used in the positive feedback loop of an op-amp, as shown in Fig. 4-7(a). A voltage divider is used in the negative feedback loop. The Wien-bridge oscillator circuit can be viewed as a noninverting amplifier configuration with the input signal fed back from the output through the lead-lag circuit. Recall that the closed-loop gain of the amplifier is determined by the voltage divider.

$$A = 1 + \frac{R_1}{R_2}$$

The circuit is redrawn in Fig. 4-7(b) to show that the op-amp is connected across the bridge circuit. One leg of the bridge is the lead-lag circuit, and the other is the voltage divider.



(a) (b)

Fig. 4-7

The unity-gain condition in the feedback loop is met when

$$A = \frac{1}{B} = \frac{1}{1/3} = 3$$

This offsets the 1/3 attenuation of the lead-lag circuit, thus making the total gain around the positive feedback loop equal to 1. To achieve a closed-loop gain of 3,

$$R_1 = 2R_2$$

Then

$$A = 1 + \frac{R_1}{R_2} = 1 + \frac{2R_2}{R_2} = 3$$

The circuit in Fig. 4-8 illustrates a method for achieving sustained oscillations. Notice that the voltage-divider circuit has been modified to include an additional resistor R_3 in parallel with a back-to-back zener diode arrangement. When dc power is first applied, both zener diodes appear as opens. This places R_3 in series with R_1, thus increasing the closed-loop gain of the amplifier as follows ($R_1 = 2R_2$):

$$A = 1 + \frac{R_1+R_3}{R_2} = 1 + \frac{2R_2+R_3}{R_2} = 3 + \frac{R_3}{R_2}$$

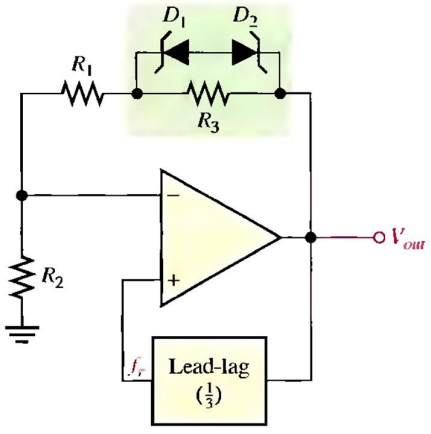


Fig. 4-8

Another method to control the gain uses a JFET as a voltage-controlled resistor in a negative feedback path. This method can produce an excellent sinusoidal waveform that is stable. A JFET operating with a small or zero V_{DS} is operating in the ohmic region. As the gate voltage increases, the drain-source resistance increases. If the JFET is placed in the negative feedback path, automatic gain control (AGC) can be achieved because of this voltage controlled resistance.

A JFET stabilized Wien bridge is shown in Fig. 4-9. The gain of the op-amp is controlled by the components shown in the dark box, which include the JFET. The JFET's drain-source resistance depends on the gate voltage. With no output signal, the gate is at zero volts, causing the drain-source resistance to be at the minimum. With this condition, the loop gain is greater than 1. Oscillations begin and rapidly build to a large output signal. Negative excursions of the output signal forward-bias D_1, causing capacitor C_3 to charge to a negative voltage. This voltage increases the drain-source resistance of the JFET and reduces the gain (and hence the output). This is classic negative feedback at work. With the proper selection of components, the gain can be stabilized at the required level.

As mentioned previously, the closed-loop gain must be 3 for oscillations to be sustained. For an inverting amplifier, the gain is that of a noninverting amplifier.

$$A = \frac{1}{B} = 1 + \frac{R_f}{R_i}$$

Referring to Fig. 4-8, R_i is composed of R_3 (the source resistor) and r'_{ds}. Substituting,

$$A = 1 + \frac{R_f}{R_3 + r'_{ds}}$$

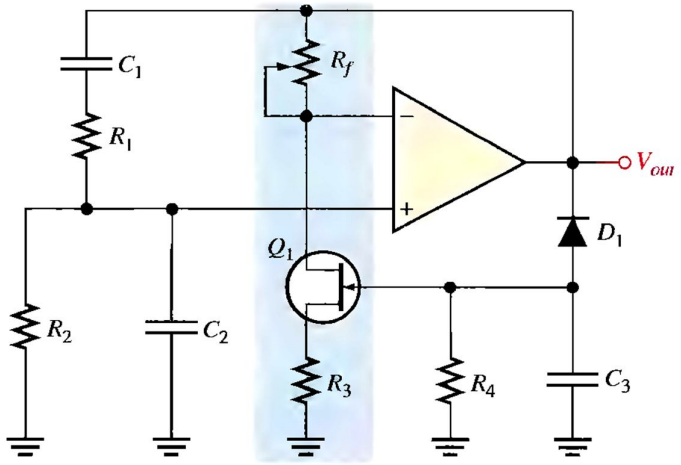


Fig. 4-9

Exercise 4-1:

(a) Determine the resonant frequency for the Wien-bridge oscillator in Fig. 4-9. Use $R_1 = R_2 = R = 10$ kΩ, $C_1 = C_2 = C = 0.01$ μF, and $R_3 = 1$ kΩ.

(b) Calculate the setting for R_f assuming the internal drain-source resistance, r'_{ds}, of the JFET is 500 Ω when oscillations are stable.

[Answers: (a) 1.59 kHz, (b) 3 kΩ]

4.3.2 Phase-Shift Oscillators:

Fig. 4-10 shows a sinusoidal feedback oscillator called the ***phase-shift*** oscillator. Each of the three RC circuits in the feedback loop can provide a maximum phase shift approaching 90°. Oscillation occurs at the frequency where the total phase shift through the three RC circuits is 180°. The inversion of the op-amp itself provides the additional 180° to meet the requirement for oscillation of a 360° (or 0°) phase shift around the feedback loop.

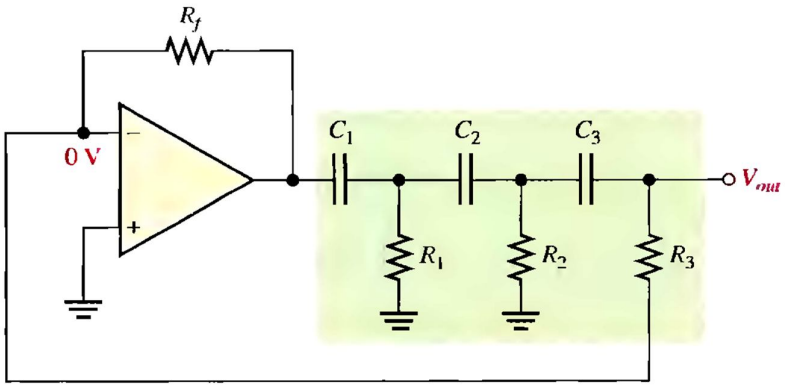


Fig. 4-10

The attenuation, B, of the three-section RC feedback circuit is:

$$B = \frac{1}{29} \qquad [4\text{-}3]$$

where $B = 1/A = R_3/R_f$

To meet the greater-than-unity loop gain requirement, the closed-loop voltage gain of the op-amp must be greater than 29 (set by R_f and R_3). The frequency of oscillation (f_r) is stated in the following equation:

$$f_r = \frac{1}{2\sqrt{6}\pi RC} \qquad [4\text{-}4]$$

where $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$.

Exercise 4-2:

(a) Determine the value of R_f necessary for the circuit in Fig. 4-10 to operate as an oscillator. Use $R_1 = R_2 = R_3 = R = 10$ kΩ and $C_1 = C_2 = C_3 = C = 0.001$ μF.

(b) Calculate the frequency of oscillation.

[Answers: (a) 290 kΩ, (b) 5.6 kHz]

Derivations of Selected Equations:

Equations 4-1 and 4-2:

$$\frac{V_{out}}{V_{in}} = \frac{R(-jX)/(R - jX)}{(R - jX) + R(-jX)/(R - jX)} = \frac{R(-jX)}{(R - jX)^2 - jRX}$$

Multiplying the numerator and denominator by j,

$$\frac{V_{out}}{V_{in}} = \frac{RX}{j(R - jX)^2 + RX} = \frac{RX}{RX + j(R^2 - j2RX - X^2)}$$

$$= \frac{RX}{RX + jR^2 + 2RX - jX^2} = \frac{RX}{3RX + j(R^2 - X^2)}$$

For a 0° phase angle there can be no j term. Recall from complex numbers in ac theory that a *nonzero* angle is associated with a complex number having a j term. Therefore, at f_r the j term is 0.

$$R^2 - X^2 = 0$$

Thus,

$$\frac{V_{out}}{V_{in}} = \frac{RX}{3RX}$$

Cancelling yields

$$\frac{V_{out}}{V_{in}} = \frac{1}{3}$$

$$R^2 - X^2 = 0$$
$$R^2 = X^2$$
$$R = X$$

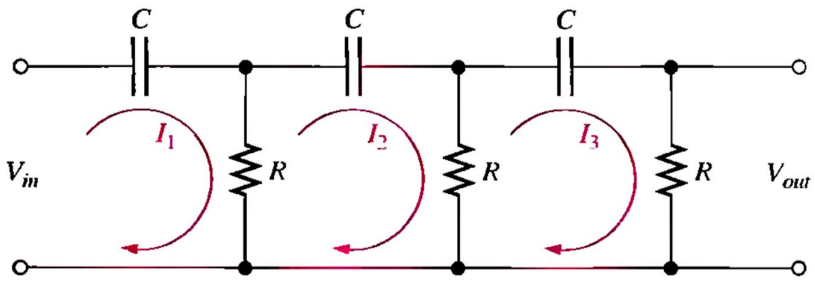
Since $X = \dfrac{1}{2\pi f_r C}$,

$$R = \frac{1}{2\pi f_r C}$$

$$f_r = \frac{1}{2\pi RC}$$

Equations 4-3 and 4-4:

The feedback circuit in the phase-shift oscillator consists of three *RC* stages, An expression for the attenuation is derived using the mesh analysis method for the loop assignment shown. All *R*s are equal in value, and all *C*s are equal in value.



$$
\begin{aligned}
(R - j1/2\pi fC)I_1 - RI_2 + 0I_3 &= V_{in} \\
-RI_1 + (2R - j1/2\pi fC)I_2 - RI_3 &= 0 \\
0I_1 - RI_2 + (2R - j1/2\pi fC)I_3 &= 0
\end{aligned}
$$

In order to get V_{out}, we must solve for I_3 using determinants:

$$
I_3 = \frac{\begin{vmatrix} (R - j1/2\pi fC) & -R & V_{in} \\ -R & (2R - j1/2\pi fC) & 0 \\ 0 & -R & 0 \end{vmatrix}}{\begin{vmatrix} (R - j1/2\pi fC) & -R & 0 \\ -R & (2R - j1/2\pi fC) & -R \\ 0 & -R & (2R - j1/2\pi fC) \end{vmatrix}}
$$

$$
I_3 = \frac{R^2 V_{in}}{(R - j1/2\pi fC)(2R - j1/2\pi fC)^2 - R^2(2R - j1/2\pi fC) - R^2(R - 1/2\pi fC)}
$$

$$
\frac{V_{out}}{V_{in}} = \frac{RI_3}{V_{in}}
$$

$$
= \frac{R^3}{(R - j1/2\pi fC)(2R - j1/2\pi fC)^2 - R^3(2 - j1/2\pi fRC) - R^3(1 - 1/2\pi fRC)}
$$

$$
= \frac{R^3}{R^3(1 - j1/2\pi fRC)(2 - j1/2\pi fRC)^2 - R^3[(2 - j1/2\pi fRC) - (1 - j1/2\pi fRC)]}
$$

$$
= \frac{R^3}{R^3(1 - j1/2\pi fRC)(2 - j1/2\pi fRC)^2 - R^3(3 - j1/2\pi fRC)}
$$

$$
\frac{V_{out}}{V_{in}} = \frac{1}{(1 - j1/2\pi fRC)(2 - j1/2\pi fRC)^2 - (3 - j1/2\pi fRC)}
$$

Expanding and combining the real terms and the j terms separately.

$$
\frac{V_{out}}{V_{in}} = \frac{1}{\left(1 - \frac{5}{4\pi^2 f^2 R^2 C^2}\right) - j\left(\frac{6}{2\pi fRC} - \frac{1}{(2\pi f)^3 R^3 C^3}\right)}
$$

For oscillation in the phase-shift amplifier, the phase shift through the *RC* circuit must equal 180°. For this condition to exist, the *j* term must be 0 at the frequency of oscillation f_r.

$$\frac{6}{2\pi f_r RC} - \frac{1}{(2\pi f_r)^3 R^3 C^3} = 0$$

$$\frac{6(2\pi)^2 f_r^2 R^2 C^2 - 1}{(2\pi)^3 f_r^3 R^3 C^3} = 0$$

$$6(2\pi)^2 f_r^2 R^2 C^2 - 1 = 0$$

$$f_r^2 = \frac{1}{6(2\pi)^2 R^2 C^2}$$

$$f_r = \frac{1}{2\pi\sqrt{6}RC}$$

Since the *j* term is 0,

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - \dfrac{5}{4\pi^2 f_r^2 R^2 C^2}} = \frac{1}{1 - \dfrac{5}{\left(\dfrac{1}{\sqrt{6}RC}\right)^2 R^2 C^2}} = \frac{1}{1 - 30} = -\frac{1}{29}$$

The negative sign results from the 180° inversion. Thus, the value of attenuation for the feedback circuit is

$$B = \frac{1}{29}$$

4.4 Oscillators with LC Feedback Circuits:

Although the RC feedback oscillators, particularly the Wien bridge, are generally suitable for frequencies up to about 1 MHz, LC feedback elements are normally used in oscillators that require higher frequencies of oscillation. Also, because of the frequency limitation (lower unity-gain frequency) of most op-amps, discrete transistors (BJT or FET) are often used as the gain element in LC oscillators. This section introduces several types of resonant LC feedback oscillators: the Colpitts, Clapp, Hartley, Armstrong, and crystal-controlled oscillators.

4.4.1 Colpitts Oscillators:

One basic type of resonant circuit feedback oscillator is the ***Colpitts***, named after its inventor-as are most of the others we cover here. As shown in Fig. 4-11, this type of oscillator uses an LC circuit in the feedback loop to provide the necessary phase shift and to act as a resonant filter that passes only the desired frequency of oscillation.

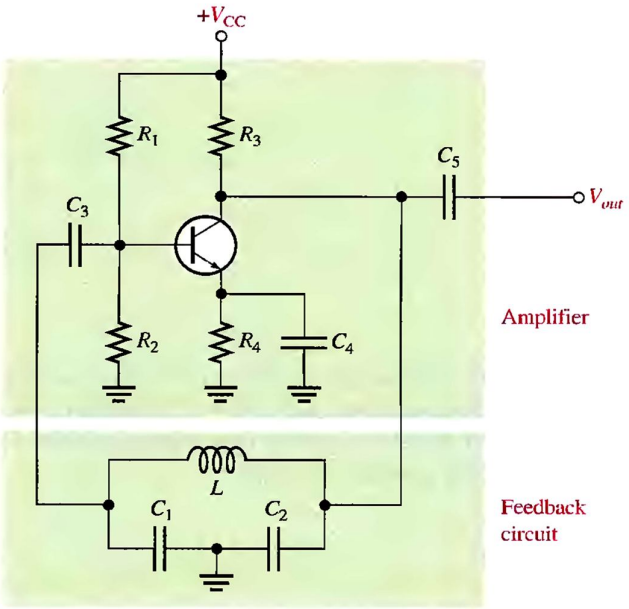


Fig. 4-11

The approximate frequency of oscillation is the resonant frequency of the LC circuit and is established by the values of C_1, C_2, and L according to this familiar formula:

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}} \qquad [4\text{-}5]$$

where C_T is the total capacitance. Because the capacitors effectively appear in series around the tank circuit, the total capacitance (C_T) is

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

The attenuation, B, of the resonant feedback circuit in the Colpitts oscillator is basically determined by the values of C_1 and C_2. Fig. 4-12 shows that the circulating tank current is through both C_1, and C_2 (they are effectively in series). The voltage developed across C_2 is the oscillator's output voltage (V_{out}) and the voltage developed across C_1 is the feedback voltage (V_f), as indicated. The expression for the attenuation (B) is

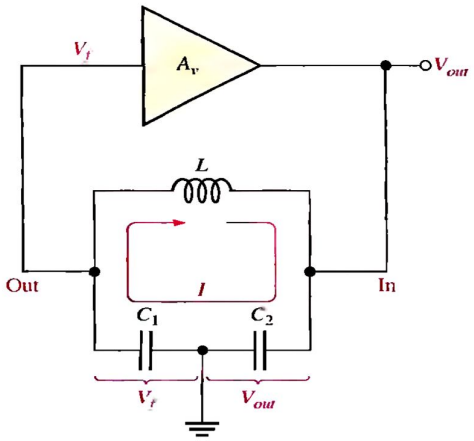


Fig. 4-12

$$B = \frac{V_f}{V_{out}} \cong \frac{IX_{C1}}{IX_{C2}} = \frac{X_{C1}}{X_{C2}} = \frac{1/(2\pi f_r C_1)}{1/(2\pi f_r C_2)}$$

Cancelling the $2\pi f_r$ terms gives

$$B = \frac{C_2}{C_1}$$

As we know, a condition for oscillation is $A_vB = 1$,

$$A_v = \frac{C_1}{C_2} \qquad [4\text{-}6]$$

where A_v, is the voltage gain of the amplifier, which is represented by the triangle in Fig. 4-12. With this condition met, $A_vB = (C_1/C_2)(C_2/C_1) = 1$. Actually, for the oscillator to be self-starting, A_vB must be greater than 1 (that is, $A_vB > 1$). Therefore, the voltage gain must be made slightly greater than C_1/C_2,

$$A_v > \frac{C_1}{C_2}$$

As indicated in Fig. 4-13, the input impedance of the amplifier acts as a load on the resonant feedback circuit and reduces the Q of the circuit. Recall from our study of resonance that the resonant frequency of a parallel resonant circuit depends on the Q, according to the following formula:

$$f_r = \frac{1}{2\pi\sqrt{LC_T}}\sqrt{\frac{Q^2}{Q^2+1}} \qquad [4\text{-}7]$$

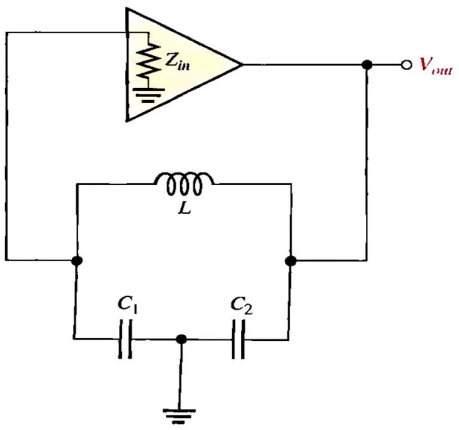


Fig. 4-13

A FET can be used in place of a BJT, as shown in Fig. 4-14, to minimize the loading effect of the transistor's input impedance. Recall that FETs have much higher input impedances than do bipolar junction transistors. Also, when an external load is connected to the oscillator output, as shown in Fig. 4-15(a), f_r, may decrease, again because of a reduction in Q. This happens if the load resistance is too small. In some cases, one way to eliminate the effects of a load resistance is by transformer coupling, as indicated in Fig. 4-15(b).

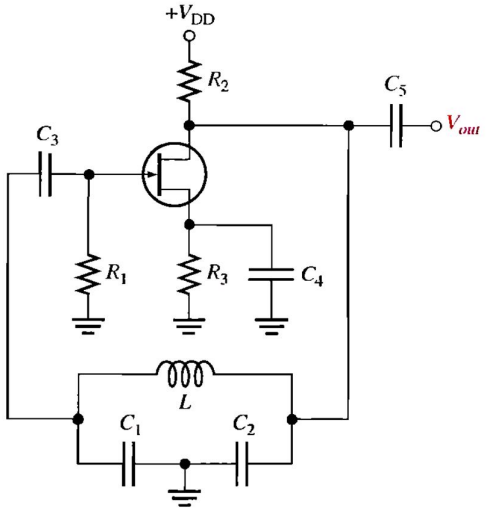
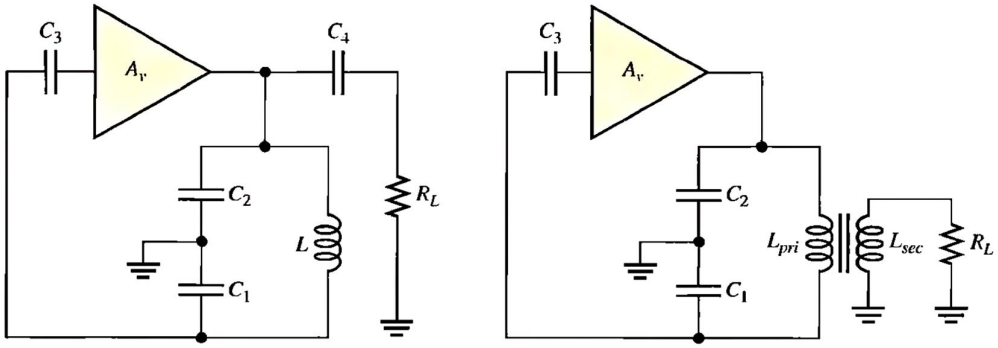


Fig. 4-14



(a) (b)

Fig. 4-15

Exercise 4-3:

(a) Determine the frequency for the oscillator in Fig. 4-11. Assume there is negligible loading on the feedback circuit and that its Q is greater than 10. Use L = 50 mH, C_1 = 0.1 µF, and C_2 = 0.01 µF.

(b) Find the frequency if the oscillator is loaded to a point where the Q drops to 8.

[Answers: (a) 7.46 kHz, (b) 7.40 kHz]

4.4.2 Clapp Oscillators:

The ***Clapp*** oscillator is a variation of the Colpitts. The basic difference is an additional capacitor, C_3, in series with the inductor in the resonant feedback circuit, as shown in Fig. 4-16. Since C_3 is in series with C_1 and C_2 around the tank circuit, the total capacitance is

$$C_T = \frac{1}{\frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3}}$$

and the approximate frequency of oscillation ($Q > 10$) is

$$f_r = \frac{1}{2\pi\sqrt{LC_T}} \qquad [4\text{-}8]$$

If C_3 is much smaller than C_1 and C_2, then C_3 almost entirely controls the resonant frequency ($f_r = 1/(2\pi\sqrt{LC_3})$). Since C_1 and C_2 are both connected to ground at one end, the junction capacitance of the transistor and other stray capacitances appear in parallel with C_1 and C_2 to ground, altering their effective values. C_3 is not affected, however, and thus provides a more accurate and stable frequency of oscillation.

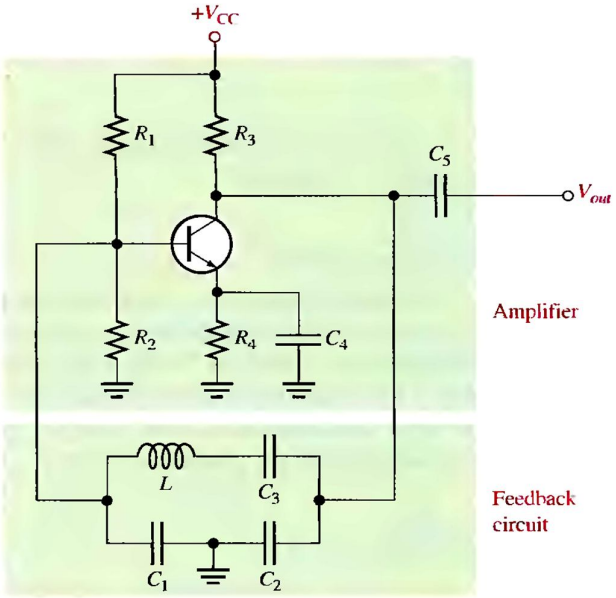


Fig. 4-16

4.4.3 Hartley Oscillators:

The ***Hartley*** oscillator is similar to the Colpitts except that the feedback circuit consists of two series inductors and a parallel capacitor as shown in Fig. 4-17.

In this circuit, the frequency of oscillation for $Q > 10$ is

$$f_r \cong \frac{1}{2\pi\sqrt{L_T C}} \qquad [4\text{-}9]$$

where $L_T = L_1 + L_2$. The inductors act in a role similar to C_1 and C_2 in the Colpitts to determine the attenuation, B, of the feedback circuit.

$$B = \frac{L_1}{L_2}$$

To assure start-up of oscillation, A_v, must be greater than $1/B$.

$$A_v > \frac{L_2}{L_1} \qquad [4\text{-}10]$$

Loading of the tank circuit has the same effect in the Hartley as in the Colpitts; that is, the Q is decreased and thus f_r decreases.

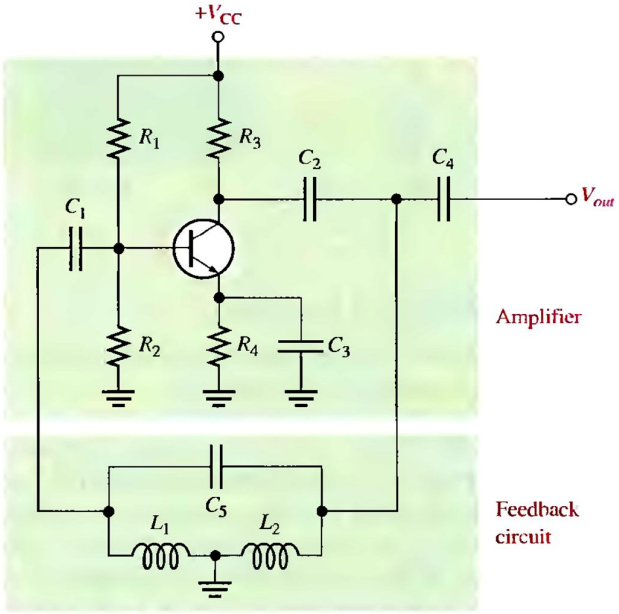


Fig. 4-17

4.4.4 Armstrong Oscillators:

This type of LC feedback oscillator uses transformer coupling to feed back a portion of the signal voltage, as shown in Fig. 4-18. It is sometimes called a "***tickler***" oscillator in reference to the transformer secondary or "tickler coil" that provides the feedback to keep the oscillation going. The ***Armstrong*** is less common than the Colpitts, Clapp, and Hartley, mainly because of the disadvantage of transformer size and cost. The frequency of oscillation is set by the inductance of the primary winding (L_{pri}) in parallel with C_1.

$$f_r = \frac{1}{2\pi\sqrt{L_{pri}C_1}} \qquad [4\text{-}11]$$

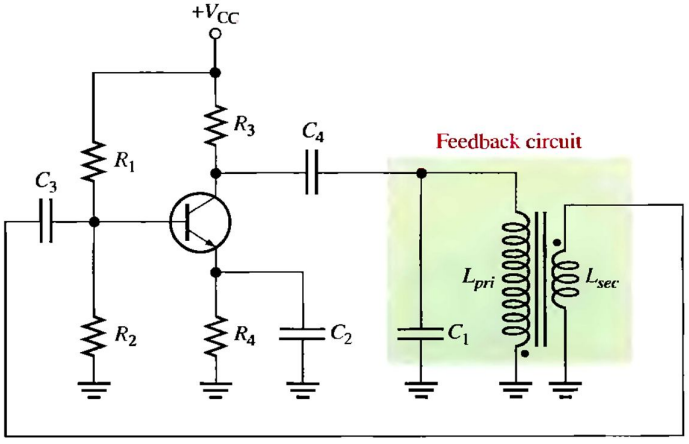
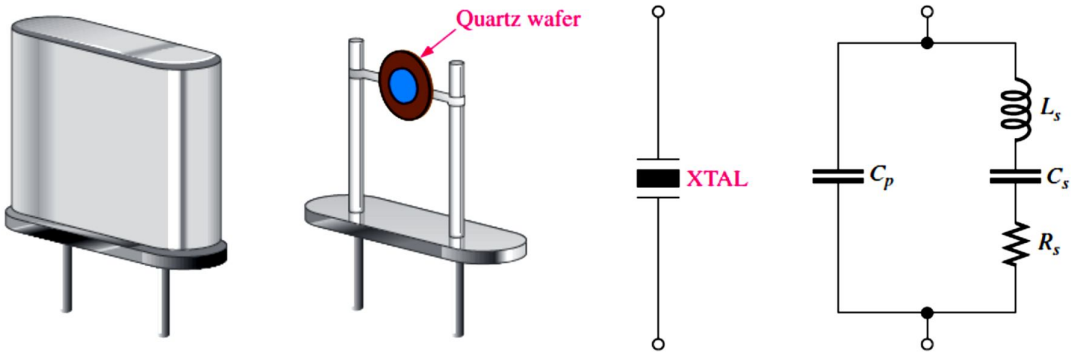


Fig. 4-18

4.4.5 Crystal-Controlled Oscillators:

The most stable and accurate type of feedback oscillator uses a ***piezoelectric crystal*** in the feedback loop to control the frequency. ***Quartz*** is one type of crystalline substance found in nature that exhibits a property called the ***piezoelectric effect***. When a changing mechanical stress is applied across the crystal to cause it to vibrate, a voltage develops at the frequency of mechanical vibration. Conversely, when an ac voltage is applied across the crystal, it vibrates at the frequency of the applied voltage. The greatest vibration occurs at the crystal's natural resonant frequency, which is determined by the physical dimensions and by the way the crystal is cut.

Crystals used in electronic applications typically consist of a quartz wafer mounted between two electrodes and enclosed in a protective "can" as shown in Fig. 4-19(a) and (b). A schematic symbol for a crystal is shown in Fig. 4-19(c), and an equivalent RLC circuit for the crystal appears in Fig. 4-19(d). The crystal's equivalent circuit is a series-parallel RLC circuit and can operate in either series resonance or parallel resonance. The impedance versus frequency of the crystal is shown in Fig. 4-20. At the series resonant frequency, f_1, the inductive reactance is cancelled by the reactance of C_s. The remaining series resistor, R_s, determines the impedance of the crystal. Parallel resonance occurs when the inductive reactance and the reactance of the parallel capacitance, C_p, are equal. The parallel resonant frequency, f_2, is usually at least 1 kHz higher than the series resonant frequency. A great advantage of the crystal is that it exhibits a very high Q (Qs with values of several thousand are typical).



(a) (b) (c) (d)

Fig. 4-19

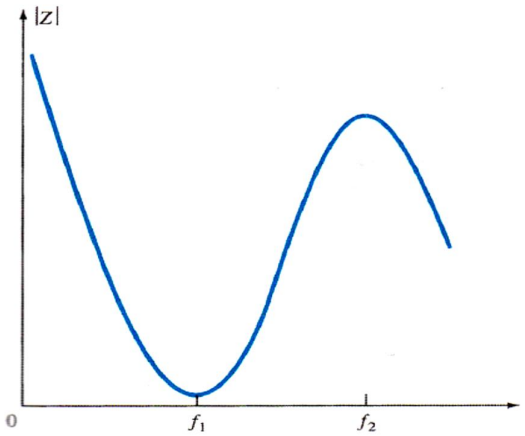


Fig. 4-20

As mentioned above, the series resonance occurs, in crystal, when $X_{Cs} = X_{Ls}$. The formula for this series resonant frequency is

$$f_1 = f_s = \frac{1}{2\pi\sqrt{LC_s}} \quad [4\text{-}12]$$

Also, the parallel resonance occurs, at higher frequency, when $X_{Cp} = X_{Ls}$. The formula for this parallel resonant frequency is

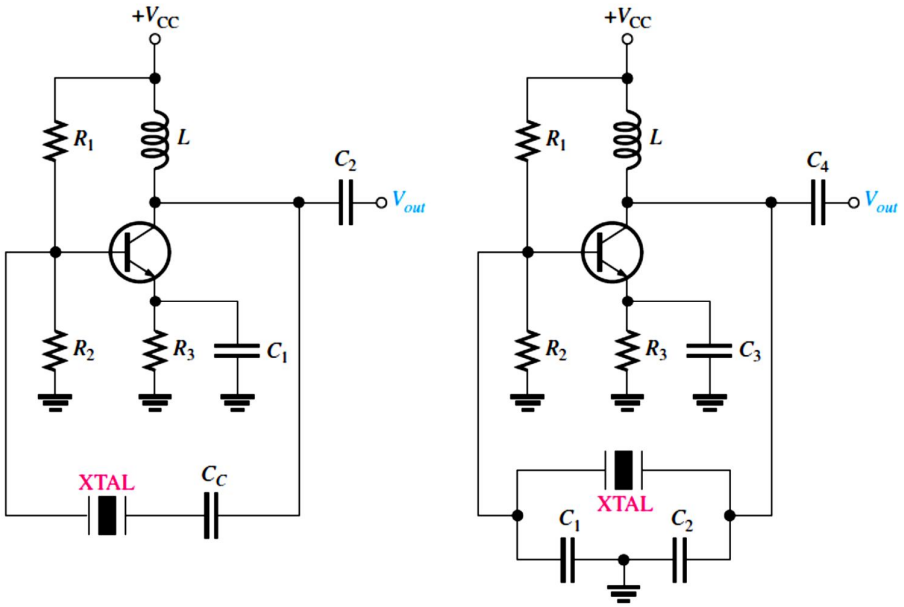
$$f_2 = f_p = \frac{1}{2\pi\sqrt{LC_T}} \quad [4\text{-}13]$$

where C_T is the series combinations of C_s and C_p, the equivalent C_T is

$$C_T = \frac{C_s C_p}{C_s + C_p}$$

An oscillator that uses a crystal as a series resonant tank circuit is shown in Fig. 4-21(a). The impedance of the crystal is minimum at the series resonant frequency, thus providing maximum feedback. The crystal tuning capacitor, C_C, is used to "fine tune" the oscillator frequency by "pulling" the resonant frequency of the crystal slightly up or down.

A modified Colpitts configuration is shown in Fig. 4-21(b) with a crystal acting as a parallel resonant tank circuit. The impedance of the crystal is maximum at parallel resonance, thus developing the maximum voltage across the capacitors. The voltage across is fed back to the input.



(a) (b)

Fig. 4-21

Piezoelectric crystals can oscillate in either of two modes-fundamental or overtone. The fundamental frequency of a crystal is the lowest frequency at which it is naturally resonant. The fundamental frequency depends on the crystal's mechanical dimensions, type of cut, and other factors, and is inversely proportional to the thickness of the crystal slab. Because a slab of crystal cannot be cut too thin without fracturing, there is an upper limit on the fundamental frequency. For most crystals, this upper limit is less than

20 MHz. For higher frequencies, the crystal must be operated in the overtone mode. Overtones are approximate integer multiples of the fundamental frequency. The overtone frequencies are usually, but not always, odd multiples (3, 5, 7, …) of the fundamental. Many crystal oscillators are available in integrated circuit packages.

Exercise 4-4:

A crystal has these values: L_s = 3 H, C_s = 0.05 pF, R_s = 2 kΩ, and C_p = 10 pF. Calculate the f_s and f_p of the crystal to three significant digits.

[Answers: 411 kHz, 412 kHz]

4.5 Relaxation (Nonsinusoidal) Oscillators:

The second major category of oscillators is the relaxation oscillator. Relaxation oscillators use an RC timing circuit and a device that changes states to generate a periodic waveform. In this section, we will learn about several circuits that are used to produce a waveform that is generally a square wave or other nonsinusoidal (triangular) waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

4.5.1 Hysteresis and Schmitt Trigger Oscillators:

Hysteresis is a property that means a device behaves differently when its input is increasing from the way it behaves when its input is decreasing. In the context of a voltage comparator, hysteresis means that the output will switch when the input increases to one level but will not switch back until the input falls below a different level. In some applications, hysteresis is a desirable characteristic because it prevents the comparator from switching back and forth in response to random noise fluctuations in the input.

Fig. 4-22(a) shows how hysteresis can be introduced into comparator operation. In this case, the input is connected to the inverting terminal and a voltage divider is connected across the noninverting terminal between v_o and a fixed reference voltage V_{REF} (which may be 0). Fig 4-22(b) shows the resulting ***transfer characteristic*** (called a ***hysteresis loop***). This characteristic shows that the output switches to $+V_{max}$ when v_{in} falls below a lower rigger level (LTL), but will not switch to $-V_{max}$ unless v_{in}, rises past an upper trigger level (UTL). The arrows indicate the portions of the characteristic followed when the input is increasing (upper line) and when it is decreasing (lower line). A comparator having this characteristic is called a ***Schmitt trigger***.

We can derive expressions for UTL and LTL using the superposition principle. Suppose first that the comparator output is shorted to ground. Then

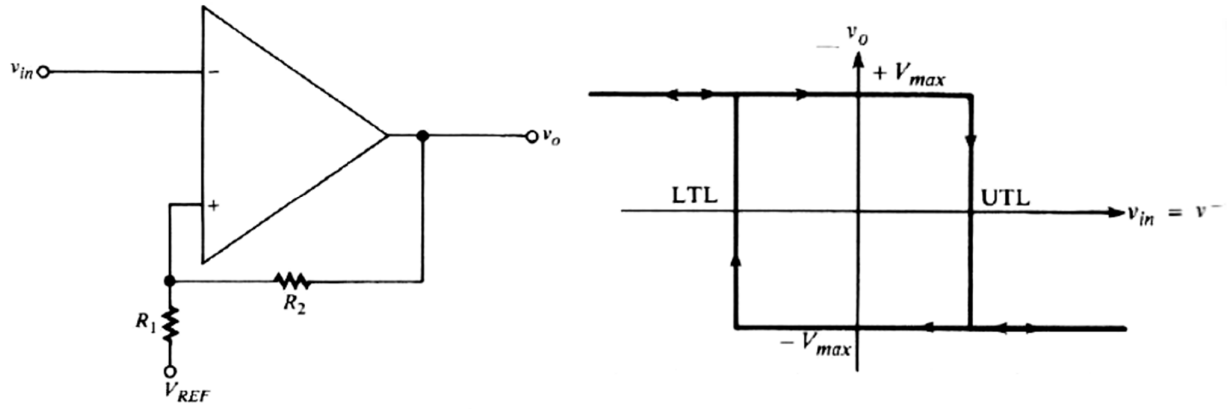
$$v^+ = \frac{R_2}{R_1+R_2}V_{REF} \quad (v_o = 0)$$

When V_{REF} is 0, we find

$$v^+ = \frac{R_1}{R_1+R_2}v_o \quad (V_{REF} = 0)$$

Therefore, when the output is at its negative limit ($v_o = -V_{max}$),

$$v^+ = \frac{R_2}{R_1+R_2}V_{REF} + \frac{R_1}{R_1+R_2}(-V_{max})$$



(a) (b)

Fig. 4-22

As can be seen in Fig. 4-22(b), v^- must ***fall***, to this value of v^+ before the comparator switches to $+V_{max}$. Therefore,

$$\text{LTL} = \frac{R_2}{R_1+R_2}V_{REF} + \frac{R_1}{R_1+R_2}(-V_{max}) \qquad [4\text{-}14]$$

Similarly, when $v_o = +V_{max}$, v_{in} must ***rise*** to

$$\text{UTL} = \frac{R_2}{R_1+R_2}V_{REF} + \frac{R_1}{R_1+R_2}(+V_{max}) \qquad [4\text{-}15]$$

In these equations, $+V_{max}$ is the maximum positive output voltage (a positive number) and $-V_{max}$ is the maximum negative output voltage (a negative number). The magnitudes of these quantities may be different; for example, $+V_{max} = 10$ V and $-V_{max} = -5$ V.

Quantitatively, the hysteresis of a Schmitt trigger is defined to be the difference between the input trigger levels. From Eqn. 4-14 and Eqn. 4-15,

$$\text{Hysteresis} = \text{UTL} - \text{LTL} = \frac{R_1}{R_1+R_2}(+V_{max}) - \frac{R_1}{R_1+R_2}(-V_{max}) \qquad [4\text{-}16]$$

If the magnitudes of the maximum output voltages are equal, we have

$$\text{Hysteresis} = \frac{2R_1V_{max}}{R_1+R_2} \qquad [4\text{-}17]$$

Exercise 4-5:

(a) Find the upper and lower trigger levels and the hysteresis of the Schmitt trigger shown in Fig. 4-23. Sketch the hysteresis loop. The output switches between ±15 V.

(b) Repeat (a) if $V_{REF} = 0$ V.

(c) Repeat (a) if $V_{REF} = 0$ V and the output switches between 0 V and +15 V.

[Answers: (a) −1V, +9V, 10V, (b) −5V, +5V, 10V, (c) 0V, +5V, 5V, Fig. 4-24]

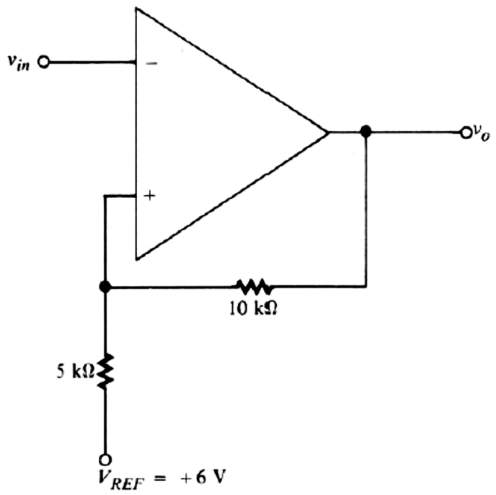


Fig. 4-23

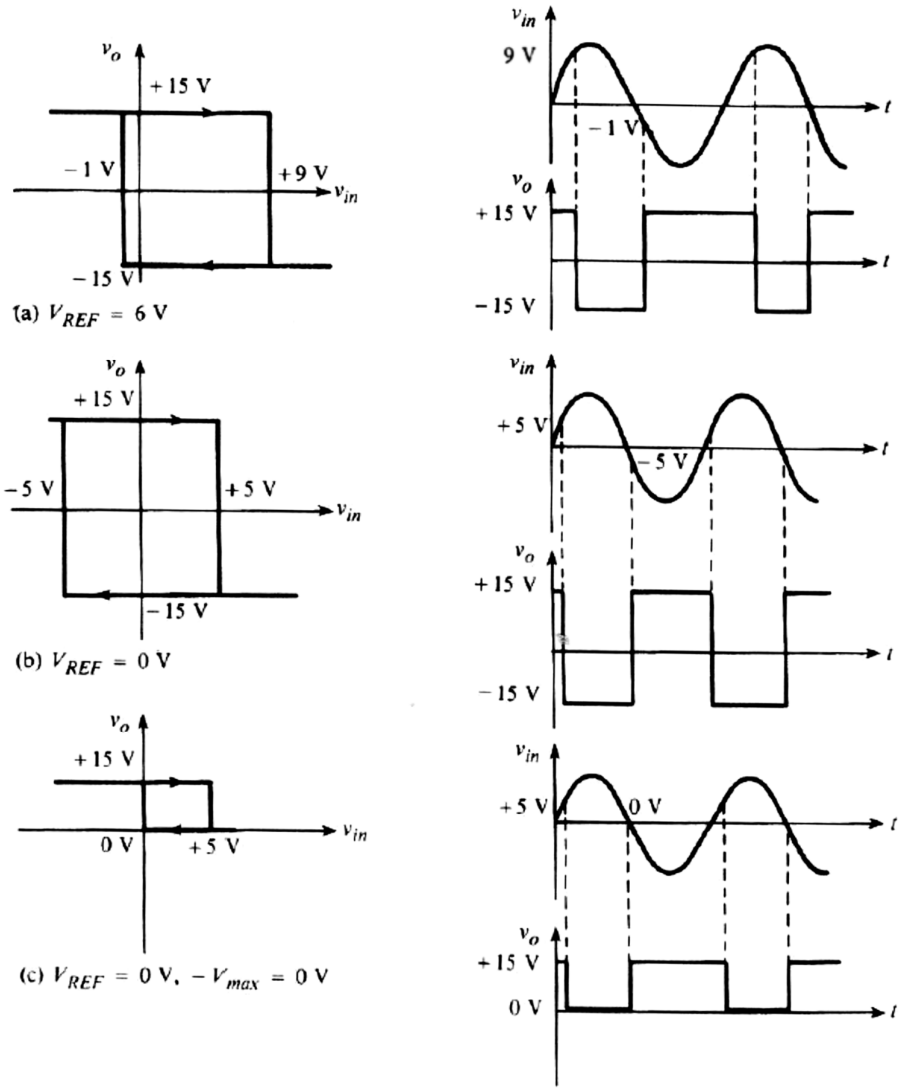
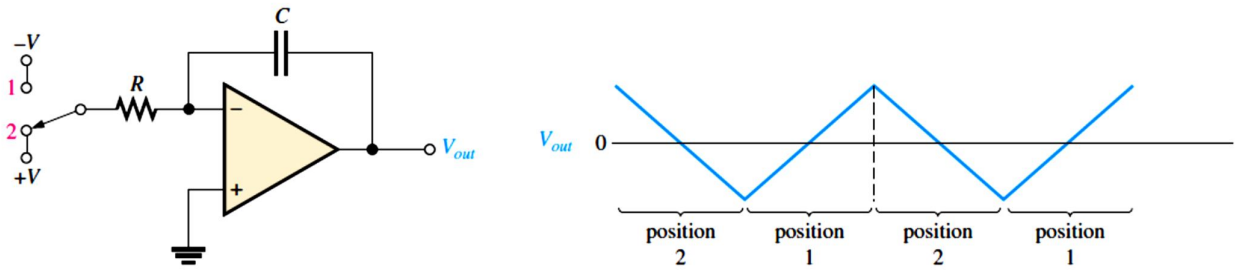


Fig. 4-24

4.5.2 A Triangular-Wave Oscillator:

The op-amp integrator can be used as the basis for a triangular-wave oscillator. The basic idea is illustrated in Fig. 4-25(a) where a dual-polarity, switched input is used. We use the switch only to introduce the concept; it is not a practical way to implement this circuit. When the switch is in position 1, the negative voltage is applied, and the output is a positive-going ramp. When the switch is thrown into position 2, a negative-going ramp is produced. If the switch is thrown back and forth at fixed intervals, the output is a triangular wave consisting of alternating positive-going and negative-going ramps, as shown in Fig. 4-25(b).



(a) (b)

Fig. 4-25

One practical implementation of a triangular wave oscillator utilizes an op-amp comparator with hysteresis to perform the switching function, as shown in Fig. 4-26. The operation is as follows. To begin, assume that the output voltage of the comparator is at its maximum negative level. This output is connected to the inverting input of the integrator through R_1, producing a positive-going ramp on the output of the integrator. When the ramp voltage reaches the upper trigger point (UTP), the comparator switches to its maximum positive level. This positive level causes the integrator ramp to change to a negative-going direction. The ramp continues in this direction until the lower trigger point (LTP) of the comparator is reached. At this point, the comparator output switches back to the maximum negative level and the cycle repeats. This action is illustrated in Fig. 4-27.

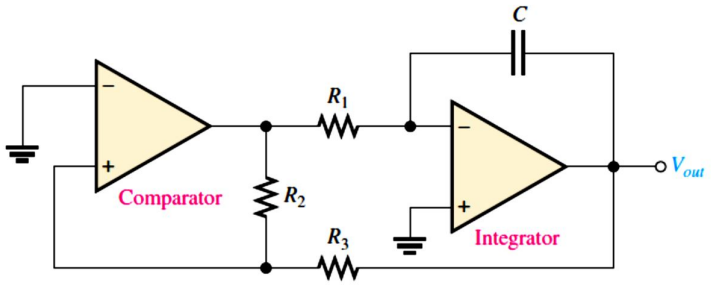


Fig. 4-26

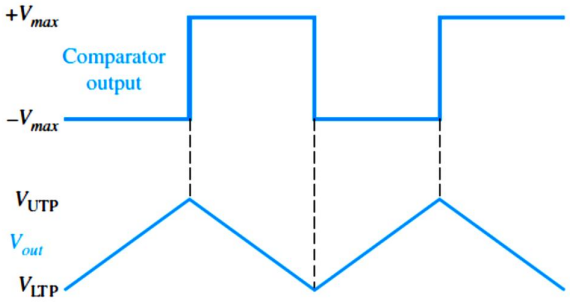


Fig. 4-27

Since the comparator produces a square-wave output, the circuit in Fig. 4-26 can be used as both a triangular-wave oscillator and a square-wave oscillator. Devices of this type are commonly known as ***function generators*** because they produce more than one output function. The output amplitude of the square wave is set by the output swing of the comparator, and the resistors R_2 and R_3 set the amplitude of the triangular output by establishing the UTP and LTP voltages according to the following formulas:

$$V_{\text{UTP}} = +V_{max}\left(\frac{R_3}{R_2}\right) \qquad [4\text{-}18]$$

$$V_{\text{LTP}} = -V_{max}\left(\frac{R_3}{R_2}\right) \qquad [4\text{-}19]$$

where the comparator output levels, $+V_{max}$ and $-V_{max}$ are equal. The frequency of both waveforms depends on the time constant as well as the amplitude-setting resistors, R_2 and R_3. By varying R_1, the frequency of oscillation can be adjusted without changing the output amplitude.

$$f_r = \frac{1}{4R_1C}\left(\frac{R_2}{R_3}\right) \qquad [4\text{-}20]$$

Exercise 4-6:

Determine the frequency of oscillation of the circuit in Fig. 4-28. To what value must R_1 be changed to make the frequency 20 kHz?

[Answers: 8.25 kHz, 4.13 kΩ]

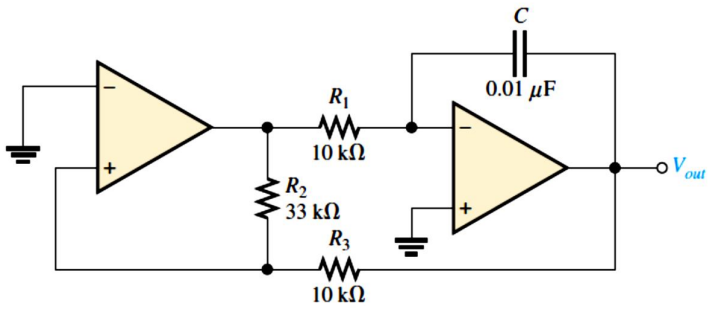


Fig. 4-28

4.5.3 A Square-Wave Oscillator (An Astable Multivibrator):

The word ***astable*** means "unstable" and, like other unstable devices, an astable multivibrator is a (***square-wave***) oscillator. (A ***bistable*** multivibrator, also called a ***flip-flop***, is a digital device with two stable states; a ***monostable*** multivibrator has one stable state, and an astable multivibrator has zero stable states.) An astable multivibrator can be constructed by using an operational amplifier as a voltage comparator in a circuit like that shown in Fig. 4-29.

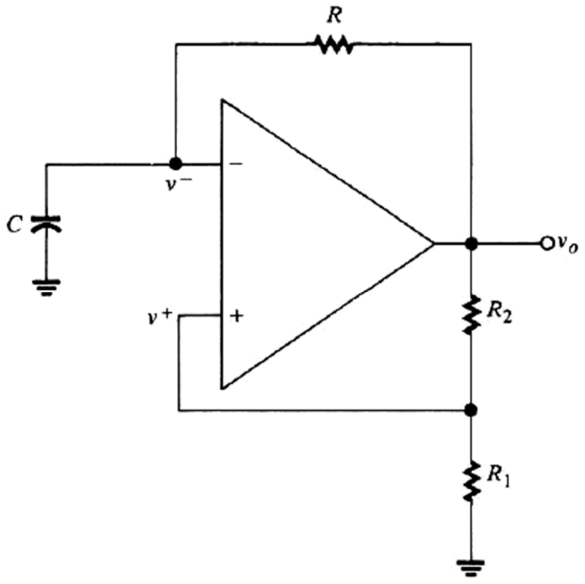


Fig. 4-29

For analysis purposes, let us assume that the output voltages of the comparator are equal in magnitude and opposite in polarity: $\pm V_{max}$. Fig. 4-30 shows the voltage across capacitor C and the output waveform produced by the comparator. We begin by assuming that the output is at $+V_{max}$. Then, the voltage fed back to the noninverting input is

$$v^+ = \frac{R_1}{R_1+R_2}(+V_{max}) = +\beta V_{max} \qquad [4\text{-}21]$$

Notice that v^- equals the voltage across the capacitor. The capacitor begins to charge through R towards a final voltage of $+V_{max}$. However, as soon as the capacitor voltage reaches a voltage equal to v^+, the comparator switches state. In other words, switching occurs at the point in time where $v^- = v^+ = +\beta V_{max}$. After the comparator switches state, its output is $-V_{max}$, and the voltage fed back to the noninverting input becomes

$$v^+ = \frac{R_1}{R_1+R_2}(-V_{max}) = -\beta V_{max} \qquad [4\text{-}22]$$

Since the comparator output is now negative, the capacitor begins to discharge through R towards $-V_{max}$. But, when that voltage falls to $-\beta V_{max}$, we once again have $v^+ = v^-$, and the comparator switches back to $+V_{max}$. This cycle repeats continuously, as shown in Fig. 4-30, with the result that the output is a square wave that alternates between $\pm V_{max}$ volts.

It can be shown that the period of the multivibrator oscillation is

$$T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right) \qquad [4\text{-}23]$$

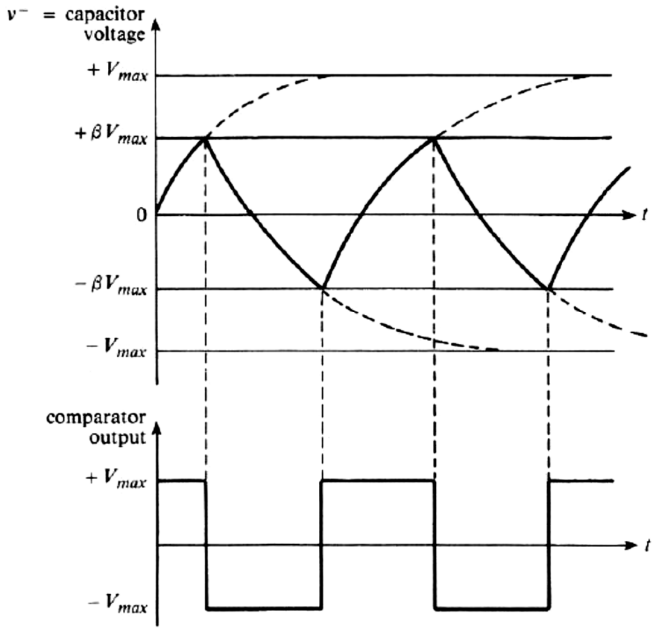


Fig. 4-30

4.5.4 The 555 Timer as an Oscillator:

The 555 timer consists basically of two comparators, a flip-flop, a discharge transistor, and a resistive voltage divider, as shown in Fig. 4-31. The flip-flop (bistable multivibrator) is a two-state device whose output can be at either a high voltage level (set, *S*) or a low voltage level (reset, *R*). The state of the output can be changed with proper input signals.

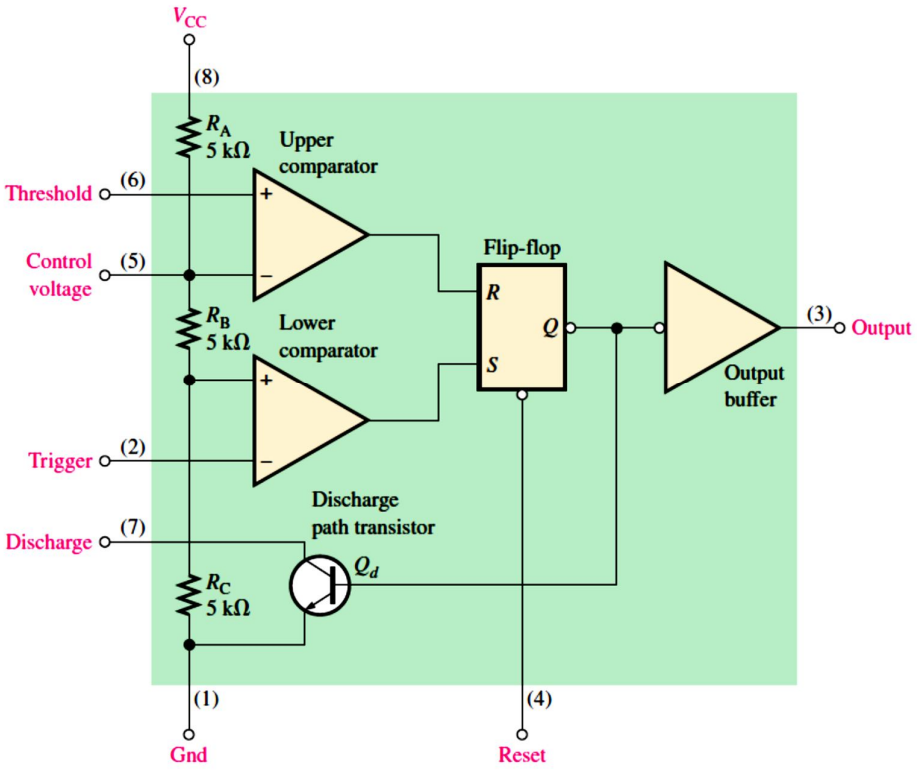


Fig. 4-31

The resistive voltage divider is used to set the voltage comparator levels. All three resistors are of equal value; therefore, the upper comparator has a reference of $^2/_3V_{CC}$, and the lower comparator has a reference of $^1/_3V_{CC}$. The comparators' outputs control the state of the flip-flop. When the trigger voltage goes below $^1/_3V_{CC}$, the flip-flop sets and the output jumps to its high level. The threshold input is normally connected to an external *RC* timing circuit. When the external capacitor voltage exceeds $^2/_3V_{CC}$, the upper comparator resets the flip-flop, which in turn switches the output back to its low level. When the device output is low, the discharge transistor (Q_d) is turned on and provides a path for rapid discharge of the external timing capacitor. This basic operation allows the timer to be configured with external components as an oscillator, a one-shot, or a time delay element.

A 555 timer connected to operate in the astable mode as a free-running relaxation oscillator (astable multivibrator) is shown in Fig. 4-32. The threshold input (THRESH) is now connected to the trigger input (TRIG). The external components R_1, R_2, and C_{ext} form the timing circuit that sets the frequency of oscillation. The 0.01 µF capacitor connected to the control (CONT) input is strictly for decoupling and has no effect on the operation.

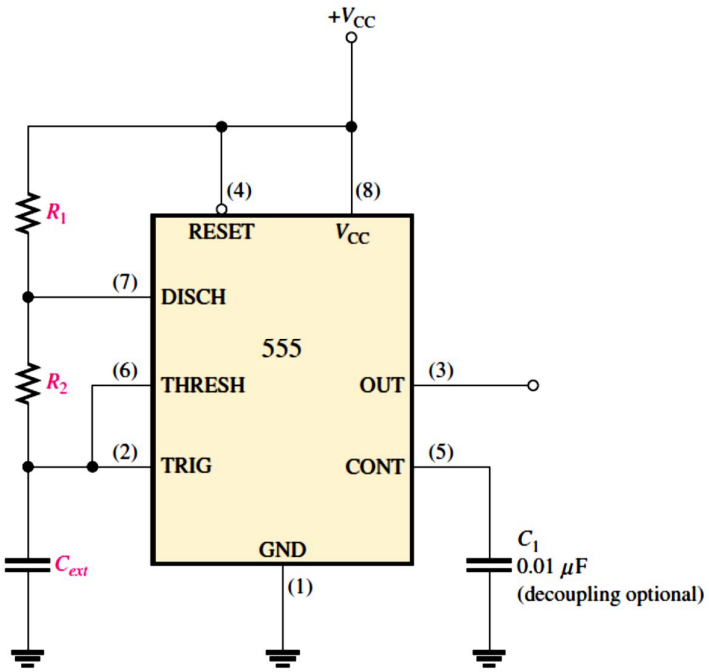


Fig. 4-32

Initially, when the power is turned on, the capacitor C_{ext}, is uncharged and thus the trigger voltage (pin 2) is at 0 V. This causes the output of the lower comparator to be high and the output of the upper comparator to be low, forcing the output of the flip-flop, and thus the base of Q_d, low and keeping the transistor off. Now, C_{ext} begins charging through $R1$ and R_2 as indicated in Fig. 4-33. When the capacitor voltage reaches $^1/_3V_{CC}$, the lower comparator switches to its low output state, and when the capacitor voltage reaches $^2/_3V_{CC}$, the upper comparator switches to its high output state. This resets the flip-flop, causes the base of Q_d to go high, and turns on the transistor. This sequence creates a discharge path

for the capacitor through R_2 and the transistor, as indicated. The capacitor now begins to discharge, causing the upper comparator to go low. At the point where the capacitor discharges down to $\frac{1}{3}V_{CC}$, the lower comparator switches high, setting the flip-flop, which makes the base of Q_d low and turns off the transistor. Another charging cycle begins, and the entire process repeats. The result is a rectangular wave output whose duty cycle depends on the values of R_1 and R_2. The frequency of oscillation is given by Eqn. 4-24, or it can be found using the graph in Fig. 4-34.

$$f_r = \frac{1.44}{(R_1+2R_2)C_{ext}} \qquad [4\text{-}24]$$

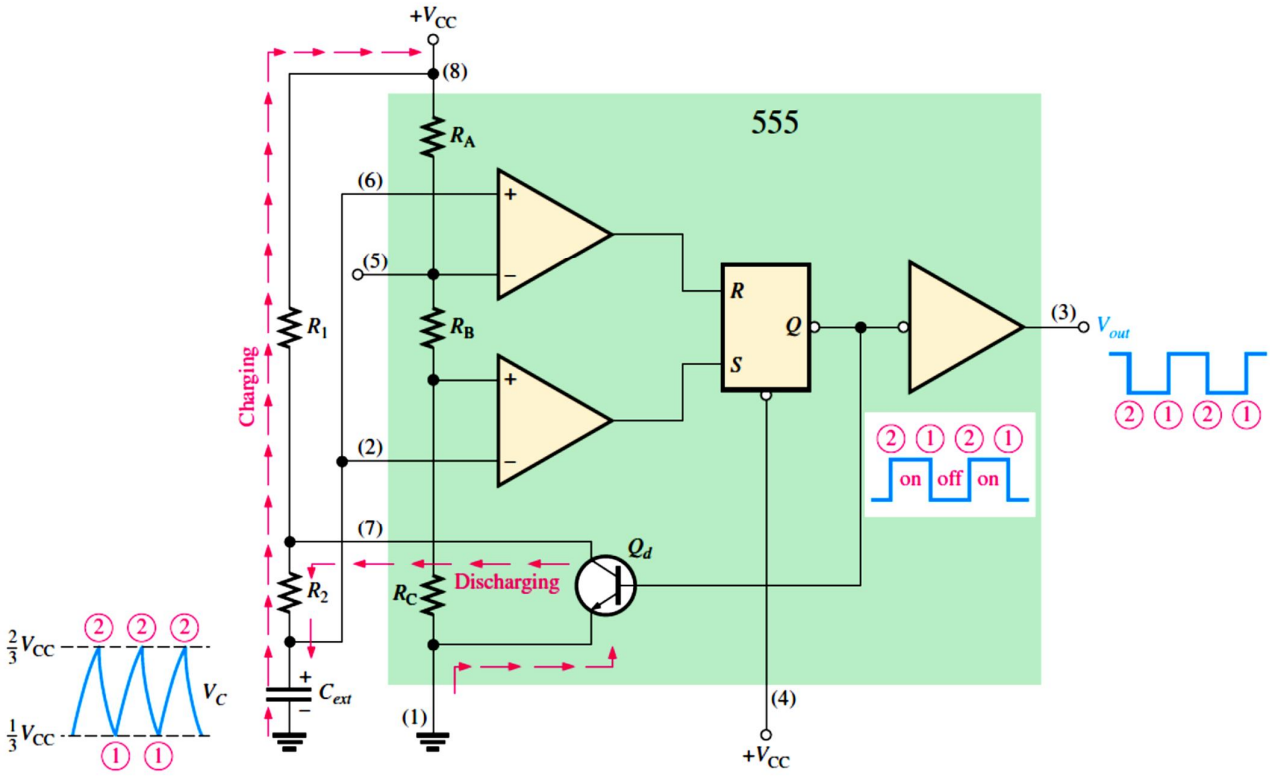


Fig. 4-33

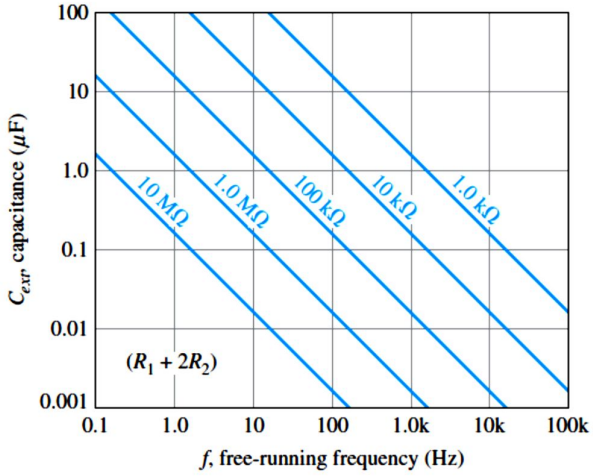


Fig. 4-34

By selecting R_1 and R_2, the duty cycle of the output can be adjusted. Since C_{ext} charges through $R_1 + R_2$ and discharges only through R_2, duty cycles approaching a minimum of 50 percent can be achieved if $R_2 >> R_1$ so that the charging and discharging times are approximately equal.

A formula to calculate the duty cycle is developed as follows. The time that the output is high (t_H) is how long it takes C_{ext} to charge from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$. It is expressed as

$$t_H = 0.694(R_1 + R_2)C_{ext} \quad [4\text{-}25]$$

The time that the output is low (t_L) is how long it takes to discharge from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$. It is expressed as

$$t_L = 0.694R_2C_{ext} \quad [4\text{-}26]$$

The period, T, of the output waveform is the sum of t_H and t_L. The following formula for T is the reciprocal of f_r in Eqn. 4-24.

$$T = \frac{1}{f_r} = t_H + t_L = 0.694(R_1 + 2R_2)C_{ext} \quad [4\text{-}27]$$

Finally, the percent duty cycle is

$$\text{Duty cycle} = \left(\frac{t_H}{T}\right)100\% = \left(\frac{t_H}{t_H + t_L}\right)100\% = \left(\frac{R_1 + R_2}{R_1 + 2R_2}\right)100\% \quad [4\text{-}28]$$

To achieve duty cycles of less than 50 percent, the circuit in Fig 4-32 can be modified so that C_{ext} charges through only R_1 and discharges through R_2. This is achieved with a diode, D_1, placed as shown in Fig. 4-35. The duty cycle can be made less than 50 percent by making R_1 less than R_2. Under this condition, the formulas for the frequency and percent duty cycle are (assuming an ideal diode)

$$f_r \cong \frac{1.44}{(R_1 + R_2)C_{ext}} \quad [4\text{-}29]$$

$$\text{Duty cycle} \cong \left(\frac{R_1}{R_1 + R_2}\right)100\% \quad [4\text{-}30]$$

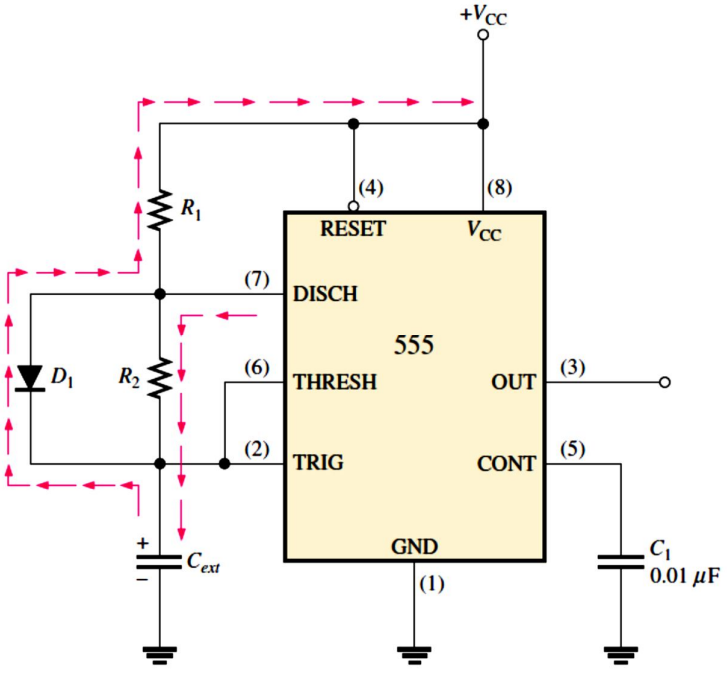


Fig. 4-35

A 555 timer can be set up to operate as a voltage-controlled oscillator (VCO) by using the same external connections as for astable operation, with the exception that a variable control voltage is applied to the CONT input (pin 5), as indicated in Fig. 4-36.

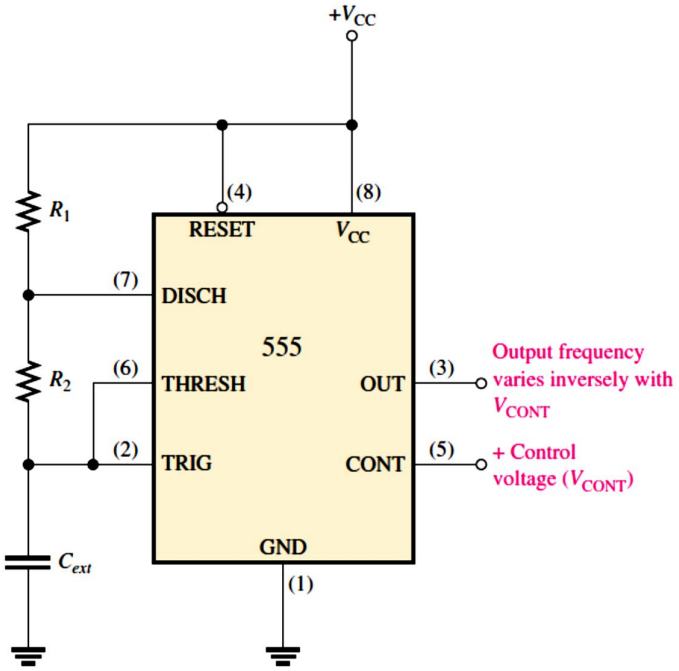


Fig. 4-36

As shown in Fig. 4-37, the control voltage (V_{CONT}) changes the threshold values of $\frac{1}{3}V_{CC}$ and $\frac{2}{3}V_{CC}$ for the internal comparators. With the control voltage, the upper value is V_{CONT} and the lower value is $\frac{1}{2}V_{CONT}$, as we can see by examining the internal diagram of the 555 timer. When the control voltage is varied, the output frequency also varies. An increase in V_{CONT} increases the charging and discharging time of the external capacitor and causes the frequency to decrease. A decrease in decreases the charging and discharging time of the capacitor and causes the frequency to increase.

An interesting application of the VCO is in phase-locked loops, which are used in various types of communication receivers to track variations in the frequency of incoming signals.

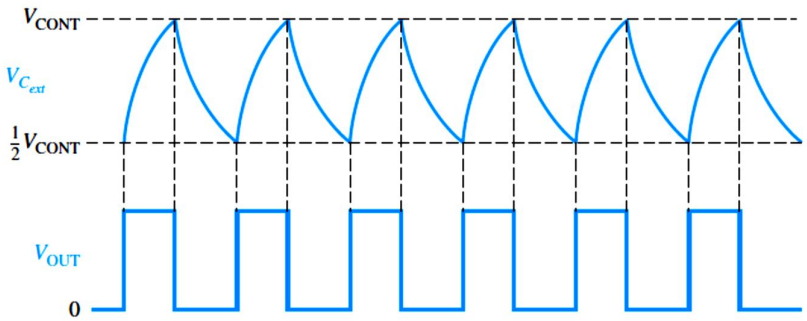


Fig. 4-37

Exercise 4-7:

A 555 timer configured to run in the astable mode (oscillator) is shown in Fig. 4-38. Determine the frequency of the output and the duty cycle.

[Answers: 5.64 kHz, 59.5%]

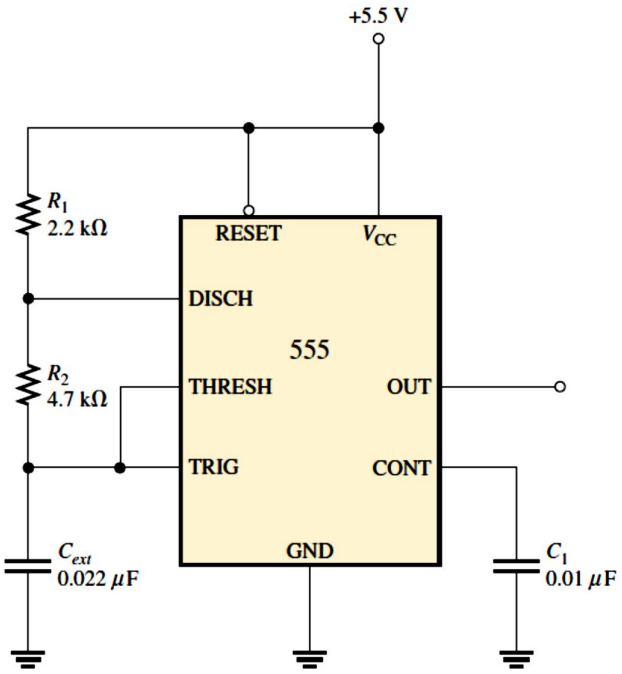


Fig. 4-38