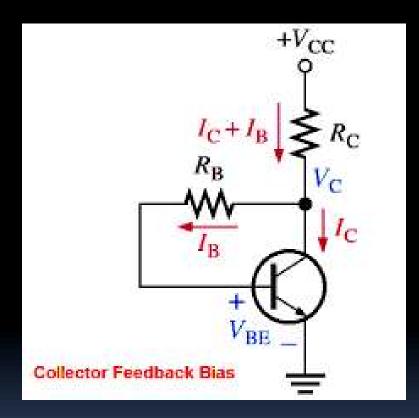
TRANSISTOR BIASING WITH EMITTER FEEDBACK Lecture-36

TDC PART -3 PAPER 6(GROUP B) Chapter -6 BY: DR. NAVIN KUMAR (ASSISTANT PROFESSOR) (GUEST FACULTY) Department of Electronics L.S COLLEGE, BRA Bihar University, Muzaffarpur.

## Transistor biasing with emitter feedback

- This type of transistor biasing configuration, often called self-emitter biasing, uses both emitter and base-collector feedback to stabilize the collector current even further.
- This is because resistors R<sub>1</sub> and R<sub>2</sub> as well as the base-emitter junction of the transistor are all effectively connected in series with the supply voltage, V.



## DEMERITS

- The downside of this emitter feedback configuration is that it reduces the output gain due to the base resistor connection.
- The collector voltage determines the current flowing through the feedback resistor, R<sub>1</sub> producing what is called "degenerative feedback".

 The polarity of this voltage reverse biases the base-emitter junction, I<sub>(current)</sub> automatically decrease. Therefore the emitter current increase less than it would have done had there been no self biasing resistor.



 This type of transistor biasing configuration works best at relatively low power supply voltages due to the configuration of "R"resistance