Junction Diode

Lecture - 13

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B.Sc (Electronics)
TDC PART - I
Paper – 1 (Group – B)
Unit – 5
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➢ Zero Applied Biased P-N Junction Diode (PART – 1)

⇨ Here in this **Lecture** we will examine the properties of the Step Junction in Thermal Equilibrium, where no currents exist and no External Excitation is applied. We will also determine here,

(1) Built-in Potential Barrier through the Depletion Layer or Space Charge Region,

(2) Electric Field and

(3) Space Charge Width

➢ (1) Built-in Potential Barrier

⇨ When no voltage is applied across the P-N Junction (i.e. with zero applied bias), the junction is in Thermal Equilibrium, the Fermi Energy Level is constant throughout the entire specimen.

⇨ The Valence Band and Conduction Band energies have to bend while moving through the Space Charge Region because the relative position of these bands with respect to the Fermi Energy changes between P – Type region and N – Type region.

⇨ Electrons in the Conduction Band of the N – Type region face a Potential Barrier when moving into the Conduction Band of the P –Type region. This Potential Barrier is known as the Built-in Potential Barrier and is denoted by $\mathbf{V_{bi}}$ or $\mathbf{V_O}$.

⇨ The Built-in Potential Barrier maintains equilibrium between Majority carrier Electrons in the N –Type region and Minority carrier Electrons in the P – Type region. It also maintains equilibrium between Majority carriers Holes in the P –Type region and Minority carrier Holes in the N – Type. The Potential Difference across the junction cannot be measured with a Voltmeter as new Potential Barriers are being formed between the semiconductor and the Probes which will cancel Built-in Potential Barrier $\mathbf{V_{bi}}$ or $\mathbf{V_O}$. **As the condition pertains** to equilibrium so no current is caused by this voltage.

⇨ The **Intrinsic Fermi Level is equidistant** from the **Conduction Band Edge through the junction**, as illustrated in the below **Figure (1).**

⇨ The **Built-in Potential Barrier** V_{bi} or V_O. is the difference between the Intrinsic Fermi Levels of the N – Type region and P –Type region written as,

$$V_{bi} = \emptyset_{Fn} + \emptyset_{Fp} \quad \text{..... (86)}$$

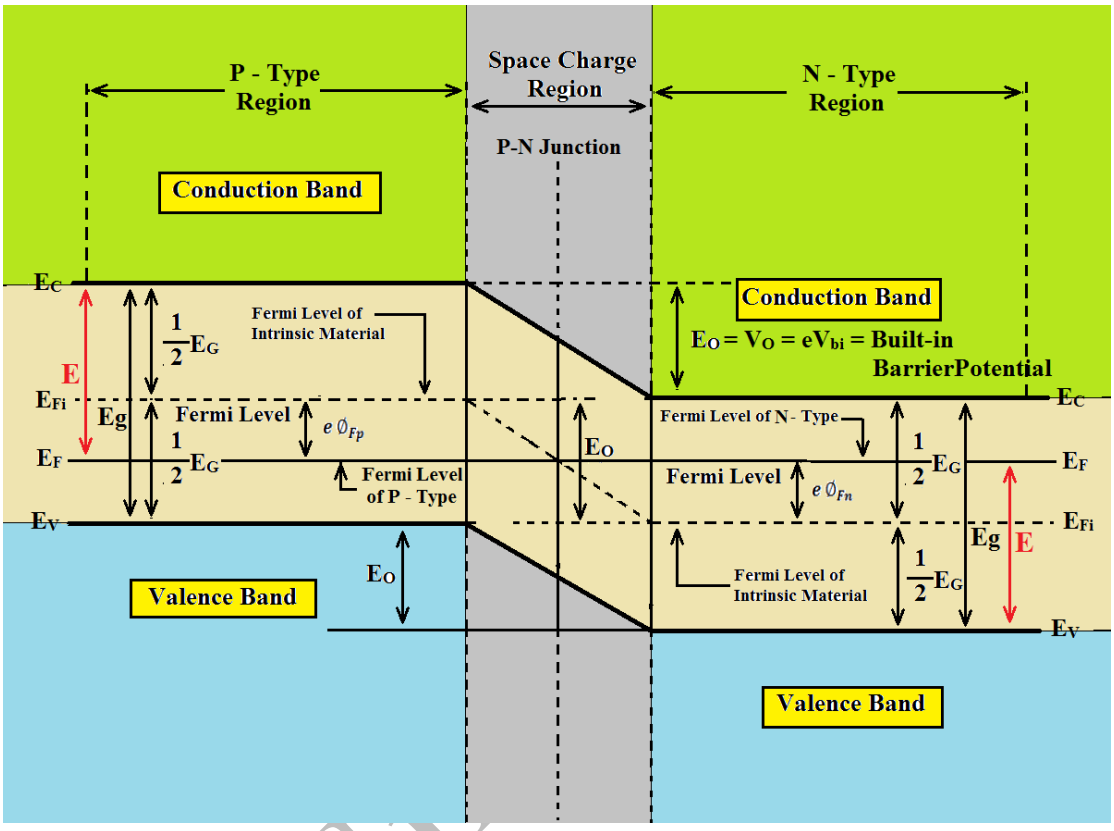

Fig. (1) Shown and illustrated that the Intrinsic Fermi Level is equidistant from the Conduction Band Edge through the junction.

⇨ The **Electron Concentration in the N – Type region Conduction Band** is written as,

$$n_o = n_C\, e^{-(E_C - E_F)/k'T} \quad \text{..... (87)}$$

$$n_o = n_i\, e^{(E_F - E_{Fi})/k'T} \quad \text{..... (88)}$$

$$\therefore\ n_o = n_i\, e^{-e\emptyset_{Fn}/k'T} \quad \text{..... (89)}$$

where, E_{Fi} and n_i are the **Intrinsic Fermi Energy** and **Intrinsic Carrier Concentration** respectively**.**

⇨ Now, **Potential $\emptyset_{Fn}$ in the N – Type region** is define as,

$$\therefore e\,\emptyset_{Fp} = e\,\emptyset_{Fn} = E_{Fi} - E_F \quad \text{..... (90)}$$

⇨ Taking **natural log of both sides** of above **Equation (89),** and setting $n_o = N_D$ we have,

$$n_o = n_i\, e^{-e\,\emptyset_{Fn}/k'T} \quad \text{..... (89)}$$

⇨ Now, we can find for the **Electron Concentration in N –Type region** by Taking **natural log of both sides** of above **Equation (89)** then we get,

$$\therefore \emptyset_{Fn} = \frac{-k'T}{e}\, log_e \frac{N_D}{n_i} \quad \text{..... (91)}$$

⇨ **Similarly from the above**, we can find for the **Hole Concentration in P –Type region**, we have,

$$\therefore \emptyset_{Fp} = \frac{-k'T}{e}\, log_e \frac{N_A}{n_i} \quad \text{..... (92)}$$

⇨ The **Built-in Potential Barrier** for the **Step Junction** is then given with help of above **Equation (86),** in which putting the value of $\emptyset_{Fn}$ the **Electron Concentration in N –Type region and** $\emptyset_{Fp}$ the **Hole Concentration in P –Type region,**

$$V_{bi} = \emptyset_{Fn} + \emptyset_{Fp} \quad \text{..... (86)}$$

$$V_{bi} = \frac{-k'T}{e} log_e \frac{N_D}{n_i} + \frac{+k'T}{e} log_e \frac{N_A}{n_i} \quad \text{..... (93)}$$

$$V_{bi} = \frac{-k'T}{e} \left(log_e \frac{N_D}{n_i} + log_e \frac{N_A}{n_i} \right) \quad \text{..... (94)}$$

$$V_{bi} = \frac{k'T}{e} log_e \frac{N_D N_A}{n_i^2} \quad \text{..... (95)}$$

$$\therefore V_{bi} = V_T log_e \frac{N_D N_A}{n_i^2} \quad \text{..... (96)}$$

where, V_T is defined as the **Thermal Voltage** and is equal to $\frac{k'T}{e}$.

⇨ In the next **Lecture - 14,** we will discuss the detailed of the **Zero Applied Biased P-N Junction Diode (PART – 2) and (2) Electric Field.**

to be continued .....

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