Paper 7, TDC Part-3
Discussion of some questions of 2018
Lecture - 2

By:

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Discussion of 2018 Questions

Q5 What is multiplexer? Design 32:1 multiplexer using two 16:1 multiplexer and one OR gate.

Sol:- Multiplexer is a special type of digital (logic) circuit that gates one out of several inputs (n) to its single output. The input selected is controlled by a set of select inputs. For selecting one out of n inputs for connection to the output, a set of m select inputs is required, where $2^m = n$. Depending upon the digital code applied at the select inputs the

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out of n data sources is selected and transmitted to a single output channel.

Normally, a strobe (enable) input is incorporated which helps in cascading and it is generally active-low, which means ~~it the output~~ selected input will present at output line when enable is low.

Depending on the no. of input lines, various size of multiplexers such as 2:1, 4:1, 8:1, 16:1 ~~and so on~~ multiplexers are available

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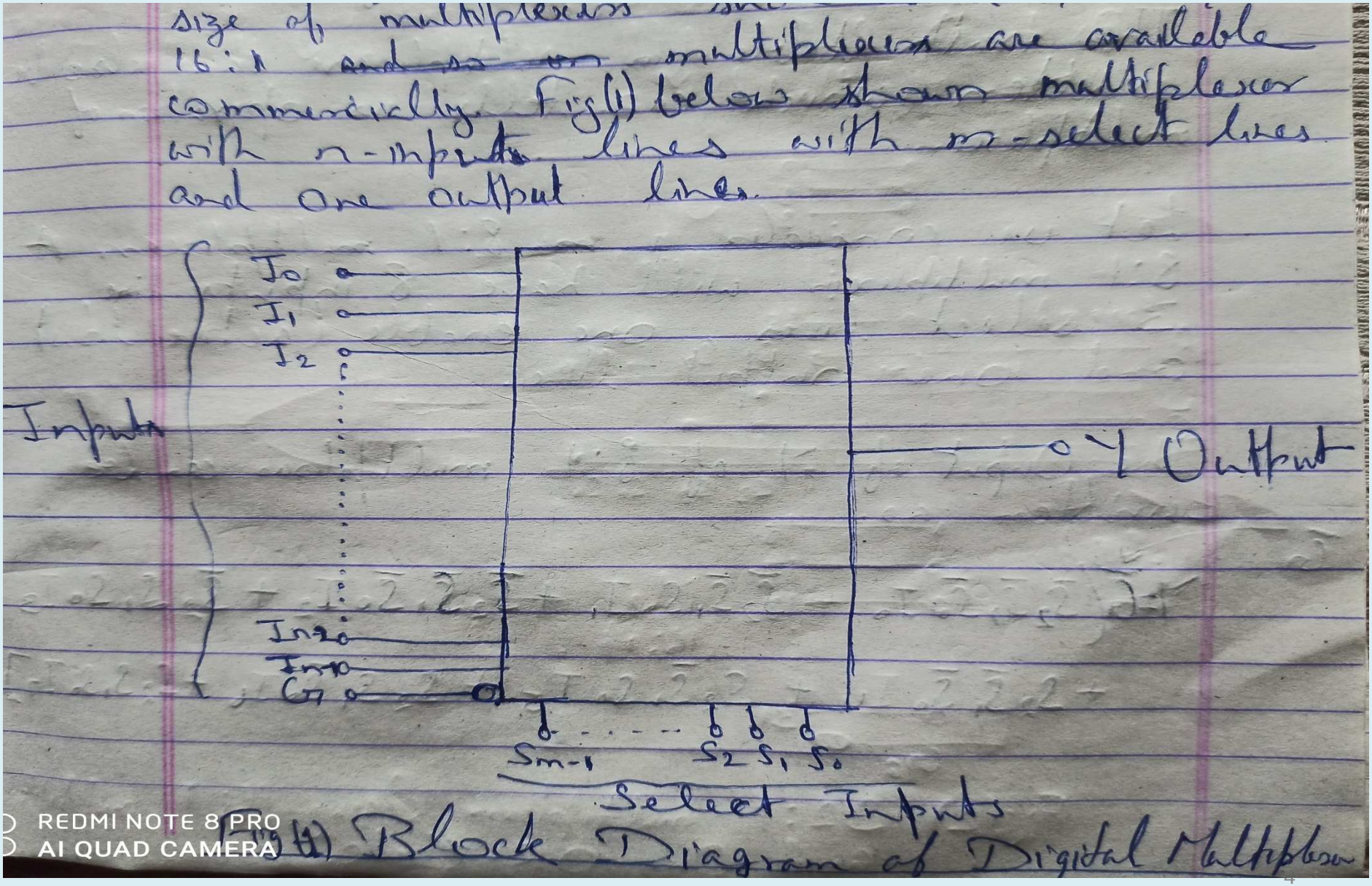

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The output Y is given by

$$Y = \overline{G}\left[\overline{S}_{m-1}\overline{S}_{m-2}\cdots\overline{S}_1\cdot\overline{S}_0\cdot I_0 + \overline{S}_{m-1}\cdot\overline{S}_{m-2}\cdots\overline{S}_1\cdot S_0\cdot I_1 + \cdots + S_{m-1}\cdot S_{m-2}\cdots S_1\cdot\overline{S}_0\, I_{n-2} + S_{m-1}\cdot S_{m-2}\cdots S_1\cdot S_0\, I_{n-1}\right] \quad \text{(i)}$$

Similarly we can write equation for output of any type of multiplexer i.e. multiplexer with any number of output.

The truth table for multiplexer can also be written which can tells us operation of

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Let us consider a 8:1 multiplexer. A 8:1 multiplexer will have 8 inputs line 3 select lines, one enable (active low) and one output line.

The Output of Y of 8:1 multiplexer can be written as.

$$Y = \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3$$
$$+ S_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

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Enable Input	Select Inputs			Output (Y)
G_1	S_2	S_1	S_0	
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2
0	0	1	1	I_3
0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7
1	X	X	X	0

Truth Table for 8:1 multiplexer.

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A 32:1 multiplexer can be designed using 16:1, since 16:1 multiplexer is the largest available IC, Therefore to meet the ~~larger input~~ 32:1 multiplexer, we use enable input and multiplexer stacks are designed.

A 32:1 multiplexer will have 32 input lines, 5 select lines & 1 output line. Fig 2 shows the design of 32:1 multiplexer using 2 nos. of 16:1 multiplexer and 1 OR-Gate.

The lower order 16 data input lines ($I_0 - I_{15}$) are applied at data input terminals of the multiplexer M_1 and the higher order 16 data i/ps

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lines ($I_{16} - I_{31}$) are applied at the data i/p terminals of the multiplexer M_2. ~~For~~ 5-select inputs are A, B, C, D, E. The most significant input bit A is applied at G_{s1} and $\bar{A}$ is applied at G_{s2}. B, C, D, & E are connected to S_3, S_2, S_1 and S_0 inputs of both the multiplexers. The o/p Y of the 32:1 multiplexer is obtained by using an OR gate

When A = 0, the Multiplexer M_1 is enabled while M_2 is disabled. When A = 1, M_2 enabled and M_1 is disabled. Remaining select input B, C, D & E will select one of the Input line of M_1 & M_2.

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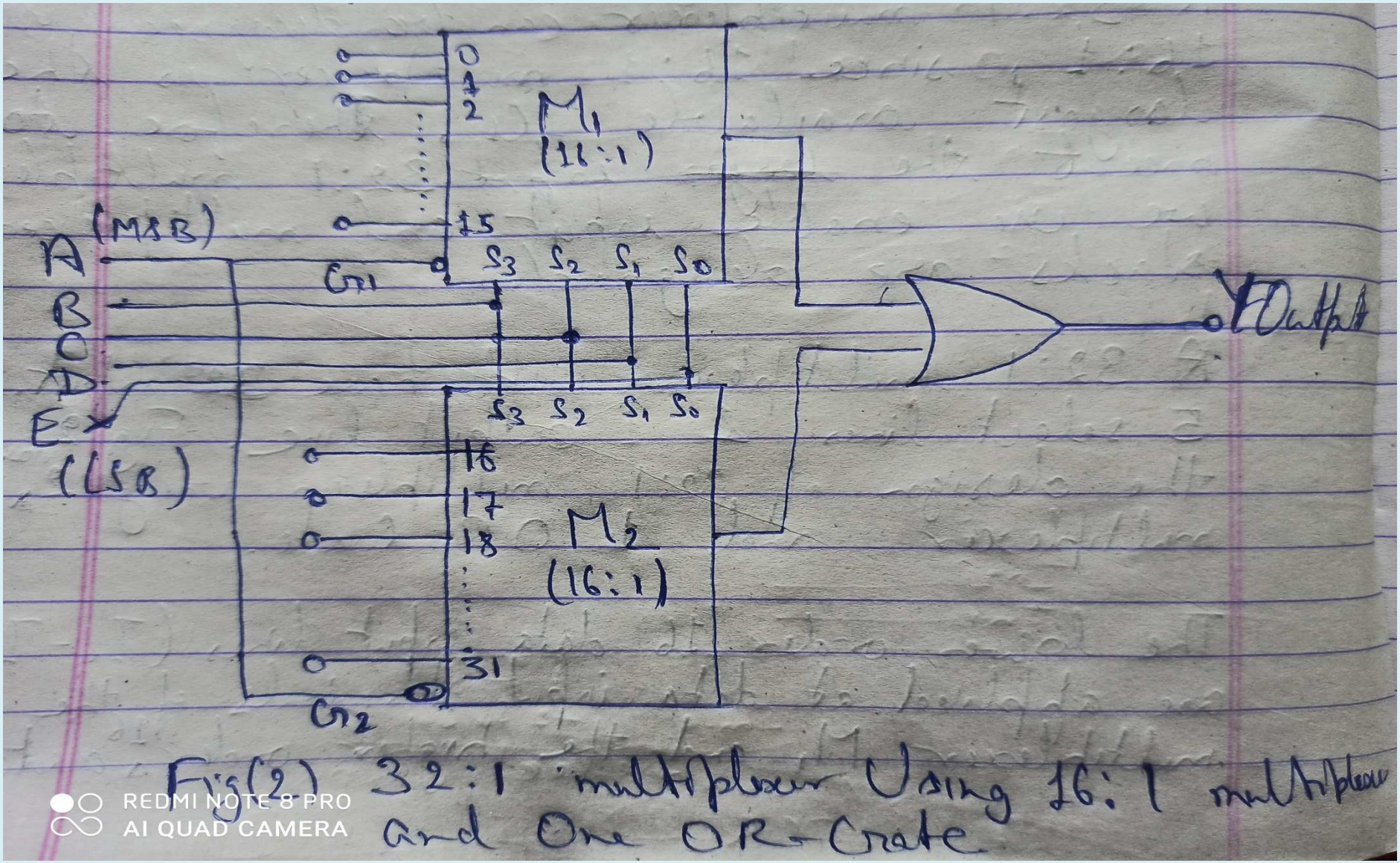

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Q7 Minimize the following logic function, using K-Map and realize the minimized function using NAND gates.

$f(A,B,C,D) = \Sigma m(1,3,5,8,9,11,15) + d(2,13)$

Sol:- The given logic function is a 4-variable function so the K-Map used to minimize this logic function will have 16 cells.

$f(A,B,C,D) = \Sigma m(1,3,5,8,9,11,15) + d(2,13$

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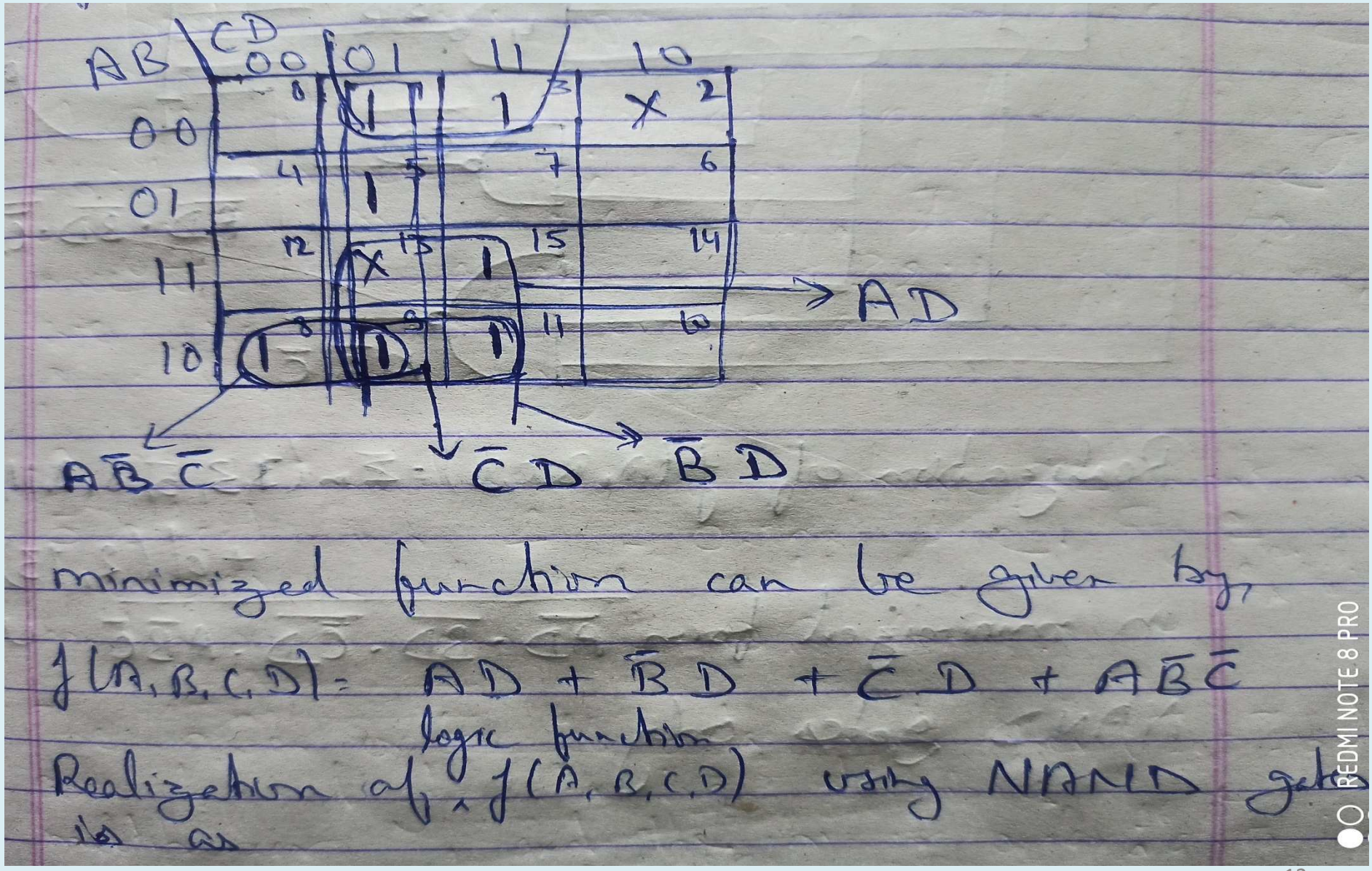

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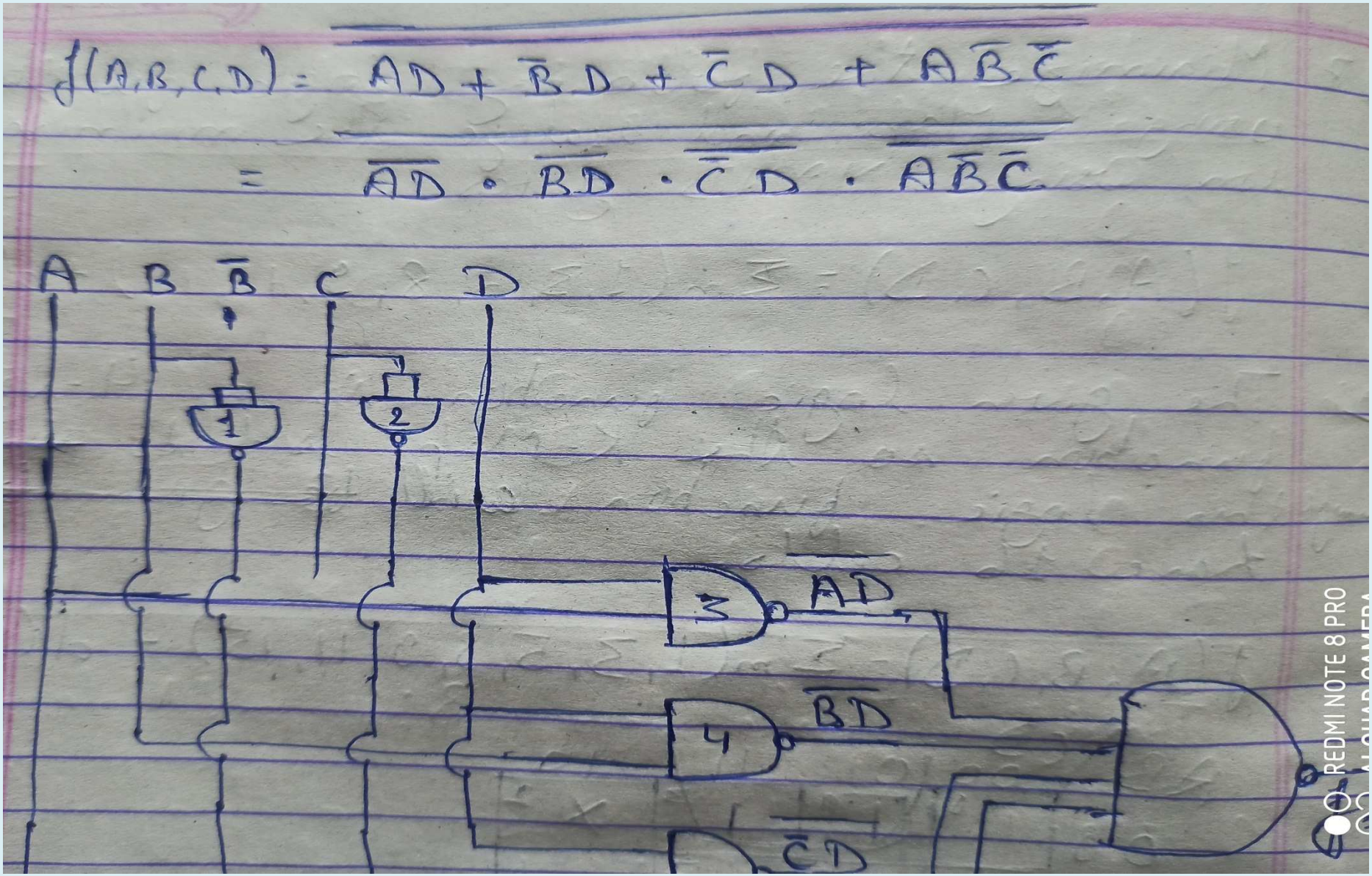

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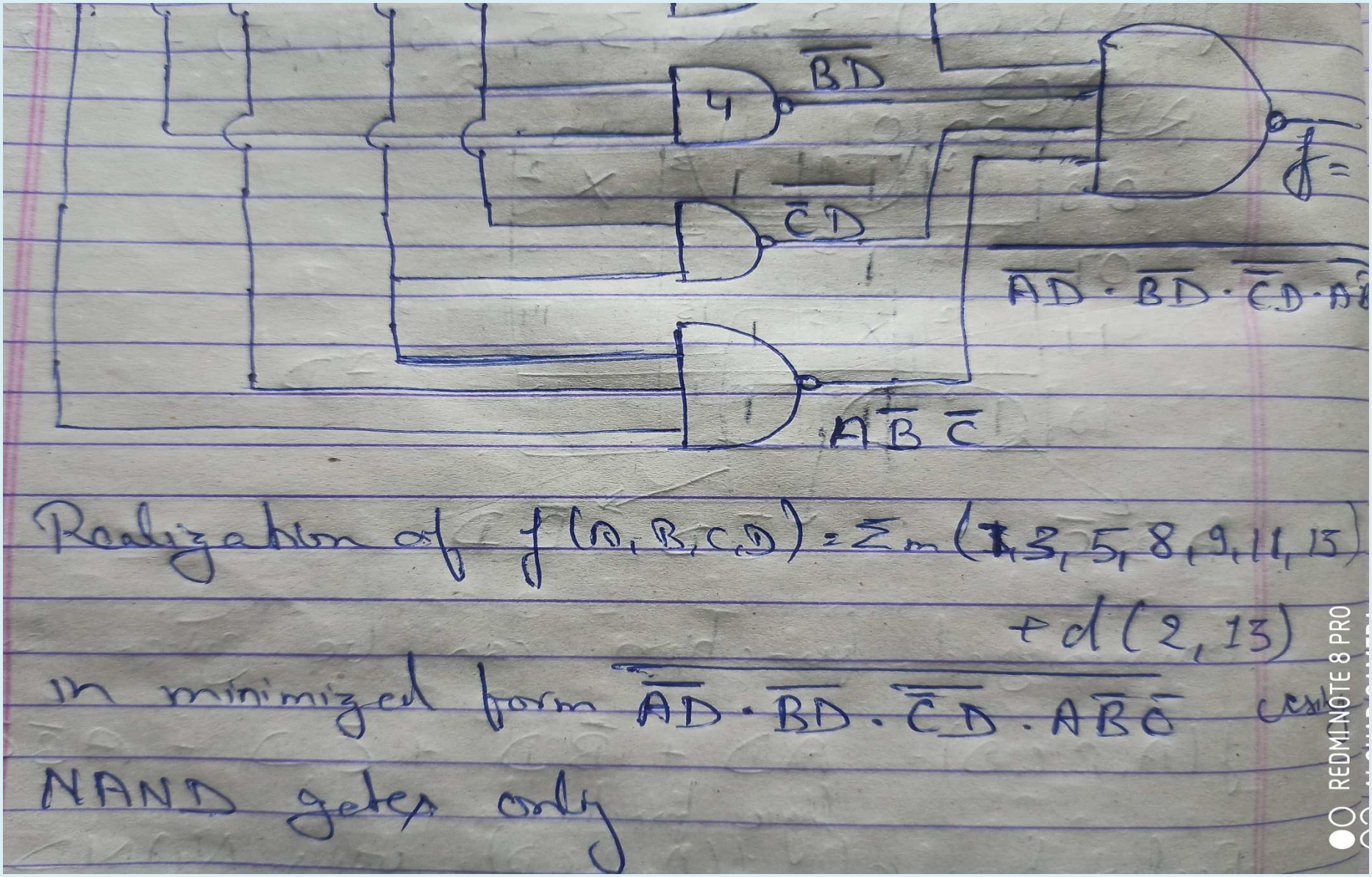

Realization of $f(A,B,C,D) = \Sigma m(1,3,5,8,9,11,15) + d(2,13)$

in minimized form $\overline{\overline{AD} \cdot \overline{BD} \cdot \overline{CD} \cdot A\overline{B}\overline{C}}$ using

NAND gates only

Combinational Logic Design

Refer book- Modern Digital Electronics by RP Jain.

Thank You