

(1)

Topic:- FET Amplifier

UG-III

Fig (1) shows a basic Common-Source FET amplifier circuit with biasing batteries. The a.c. signal to be amplified is connected ~~to~~ in series with the gate bias battery V_{GG} . This causes a variation in the total gate-to-source voltage. The load resistance R_L is connected to the drain terminal, as shown. The output voltage is measured across this resistance or across the FET. Let the output ~~voltage~~ a.c. voltage be V_{as} for an input signal voltage V_{gs} .

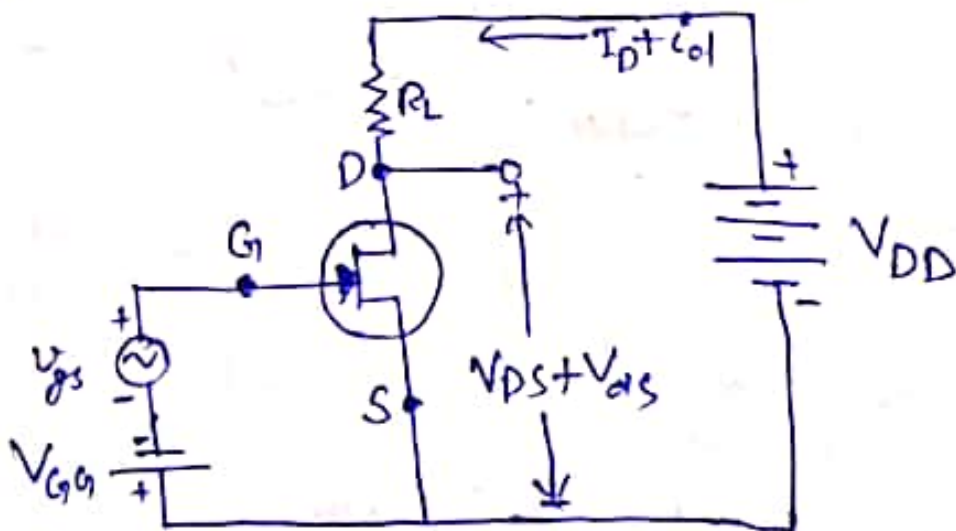


Fig (1)

(2)

When the signal voltage is positive with respect to the source, the gate becomes less negative with respect to the source. As a result, the drain current is enhanced, causing a large voltage drop across R_L which makes the drain terminal less positive with respect to the source. A small voltage variation at the gate produces a sizable voltage variation across R_L resulting in amplification. Also, since an increase of the gate voltage causes a decrease in the drain voltage, there is a phase shift of 180° between the input and the output of the FET amplifier.

Expression For Gain

Applying Kirchhoff's voltage law to the output circuit in fig (1), we get for d.c. voltages

$$V_{DD} = V_{DS} + I_D R_L \dots \dots \dots (1)$$

and for a.c. voltages

$$v_{ds} + i_d R_L = 0 \dots \dots \dots (2)$$

Also we have for the small-signal case

$$i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds} \longrightarrow (3)$$

Because, about the quiescent point we can express the a.c. component of the drain current I_d as a linear sum of v_{gs} and v_{ds} that is

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_d} \longrightarrow (4)$$

(3)

Here V_{gs} and V_{ds} stand for the a.c. components of the gate-to-source and the drain-to-source voltages, respectively. From equation (4) we can write

$$g_m = \left. \frac{i_d}{V_{gs}} \right|_{V_{ds}=0} \quad \text{It is called the "mutual conductance or trans-conductance".}$$

And $r_d = \left. \frac{V_{ds}}{i_d} \right|_{V_{gs}=0}$ & is called the a.c. drain or channel or output resistance of the FET.

($V_{ds}=0$ means V_{DS} is constant and V_{GS} is constant for now from eqⁿ (2) and (3), we have

$$V_{ds} + R_L (g_m V_{gs} + \frac{1}{r_d} V_{ds}) = 0 \quad \text{--- (5)}$$

or, $V_{ds} + R_L g_m V_{gs} + \frac{R_L}{r_d} V_{ds} = 0$

or, $(1 + \frac{R_L}{r_d}) V_{ds} = -R_L g_m V_{gs}$

or, $\frac{V_{ds}}{V_{gs}} = - \frac{R_L g_m r_d}{(R_L + r_d)}$

or, $A_V = - \frac{\mu R_L}{r_d + R_L} \quad \text{--- (6)}$

Here, $\mu = - \left. \frac{V_{ds}}{V_{gs}} \right|_{i_d=0} = r_d g_m \quad \text{--- (7)}$

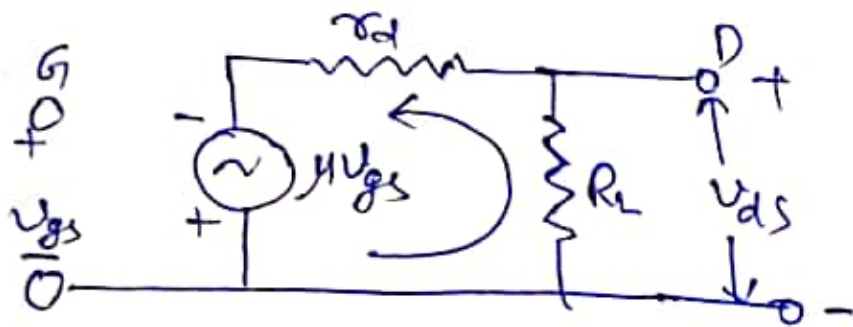
and is known as "amplification factor" of the FET. From eqⁿ (6) we have

$$V_{ds} = - \frac{\mu V_{gs} R_L}{r_d + R_L}$$

and the a.c. component of the drain current is

$$i_d = -\frac{v_{gs}}{R_L} = \frac{\mu v_{gs}}{r_d + R_L} \quad \text{---} \rightarrow \textcircled{8}$$

Eqⁿ (8) gives us a.c. voltage source equivalent circuit of the common-source FET amplifier shown in fig (2). This is equivalent to the device of voltage source μv_{gs} , in series with a resistor r_d .



Fig(2)

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