Hartley oscillator

UG-III ~ Dr. S. Roy

Hartley oscillator is a sinusoidal oscillators using a junction transistor in CE mode as shown in fig (1). The resistors R_1, R_2 and R_E, and the supply voltage V_{cc} establish the d.c. operating point. Capacitors C_B and C_E are respectively the blocking and bypass capacitors which blocks the d.c. component. The capacitor C and the inductor L_1 and L_2 form the frequency determining circuit (i.e parallel resonant circuit). The junction of L_1 and L_2 is earthed. The output is taken out of the coil L_2.

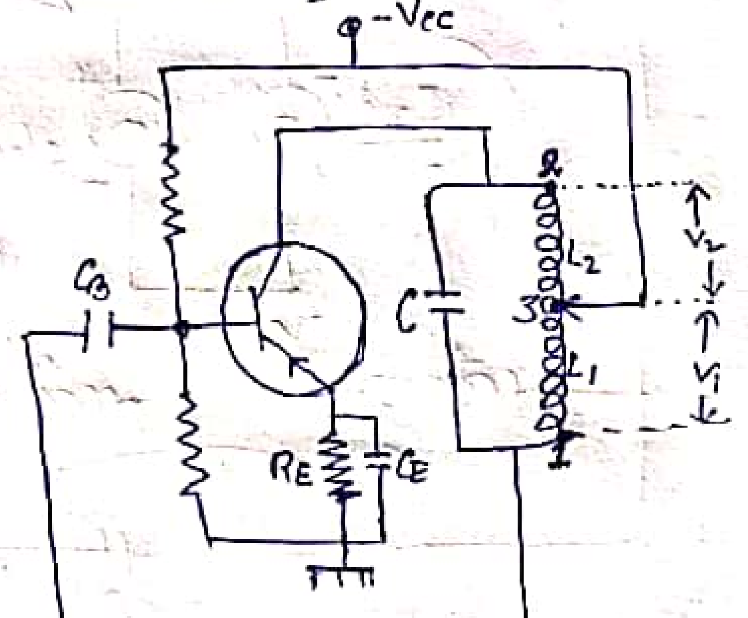

Fig (1)

Working: – To maintain sustained (continuous) oscillation, the total phase shift between input and output must be 0° or 360°. For this, a parallel resonant circuit (LC circuit) and a transistor in CE-mode are used, because each produces 180° phase shift between input and output.

When the supply voltage is switched on, a transient current is set up in the tank circuit. As a result damped harmonic oscillation are set up in the circuit. The oscillatory current produces an a.c. voltage across L_1 and another a.c. voltage across L_2. Since the junction of the coils L_1 and L_2 is earthed, it will be at zero potential. When the point 1 is at positive potential with respect to 3, the point 2 will be negative potential with respect to 3 at the same instant of time. Thus, the voltage across L_1 is feed back into the circuit. The voltage across L_2 is taken out to the output. In this way the parallel resonant circuit provides a phase difference of 180° between the output collector voltage and the feedback voltage. In CE mode the transistor introduces 180° phase difference between input and outputs. Thus the total phase shift is zero or 360° which is the necessary condition for sustained oscillation.

Analysis:- Since the bias resistances R_1, R_2 & R_E are sufficiently large, they will not affect the ac operation of the circuit. Hence the hybrid model ac equivalent circuit of the Hartley oscillator is shown in fig(2).

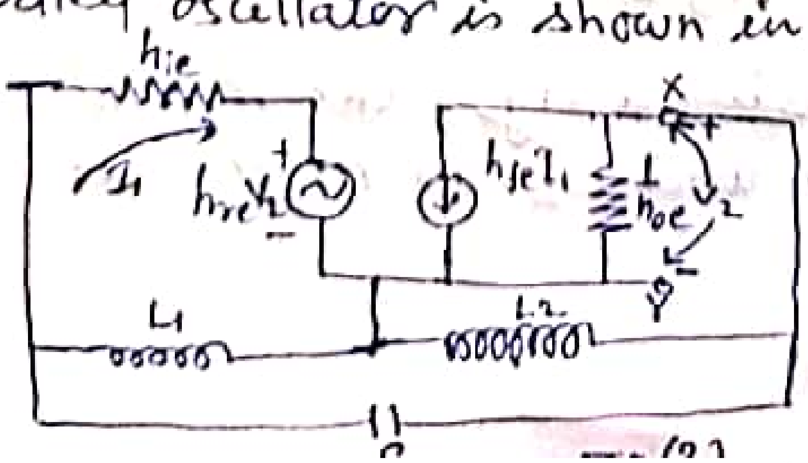

fig (2)

Applying Thevenin's theorem at the terminals X, Y in Fig (2) and looking ~~two~~ towards left, the current source $h_{fe} I_1$ in parallel with the resistance $(1/h_{oe})$ can be replaced by an equivalent Thevenin voltage source of generated voltage $(h_{fe} I_1/h_{oe})$ and internal resistance $1/h_{oe}$. This Thevenin representation is shown in fig(3).

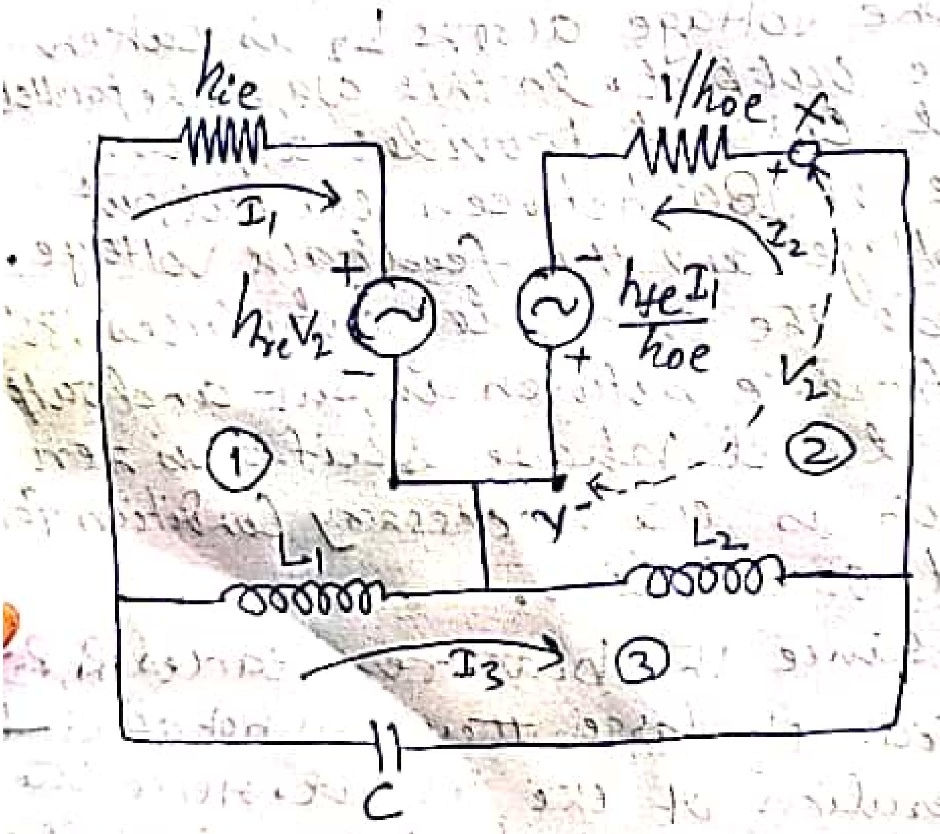

Fig (3)

For simplicity, the mutual inductance between L_1 and L_2 is neglected.